INVESTIGATION INTO HIGH EFFICIENCY DC-DC CONVERTER TOPOLOGIES FOR A DC MICROGRID SYSTEM

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Abstract

Distributed generation in the form of DC microgrids has recently attracted increasing research interest. For integrating primary sources and energy storage devices to the DC bus of a DC microgrid power electronic converters are necessary, but the associated losses may degrade the microgrid efficiency. Therefore, the aim of this work is to develop high-efficiency converters, particularly for fuel cell generators and ultracapacitors energy buffers suitable for use in a stationary distribution system. Based on the evaluation of the fuel cell dynamic performance, a current–fed DC–DC converter design with a lower voltage rating of the switching devices and a higher DC voltage conversion ratio is proposed. A number of optimisation approaches have been applied to further improve the converter efficiency over its full power range. The periodic steady state operation of the converter is analysed in detail; state-space averaging is then used to determine the small signal equations and derive transfer functions. A closed loop controller has been designed and verified by a novel PSpice/Simulink/actual processor co–simulation approach, where the modelling results are validated by experimental results using a model–based design method.

To sustain the charging and discharging states of the ultracapacitor, a bidirectional DC–DC converter is required. Based on a comprehensive overview on different DC–DC converter topologies, the research presented here has shown that, bidirectional voltage–fed topology is better suited for dealing with the fast dynamic response of the ultracapacitor. But for a wide input voltage variation, this topology exhibits a higher circulating power flow and higher conduction losses as a consequence. Therefore, a detailed analysis of the bidirectional converter exploring the impact of the circulating power flow interval is developed in this study. Analytic methods have been applied to establish the optimal operation of the bidirectional voltage–fed converter for an ultracapacitor to improve its performance and efficiency. Based on these methods, a novel modulation scheme is proposed that minimises the circulating power flow in the converter, that has been verified by detailed simulation.

I dedicate this thesis to my parents, wife and sons

Acknowledgements

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Chapter One

Introduction

1.1 State of The Art Microgrid Systems

Traditional power systems are facing a number of problems such as low energy efficiency, environmental pollution, drastic increases of the fossil fuel prices and gradual depletion of fossil fuel resources. These problems have led to the development of a new concept for power generation so as to generate electricity locally by utilising small non-conventional and renewable energy sources such as microturbines, back-up diesel generators, wind turbines, solar photovoltaic cells, and fuel cells [1]. This kind of power generation called a “distributed generation” system. In distributed generation systems the electricity is generated very close to the consumption sites. This leads to a reduction of the energy lost on long transmission lines and reduces the size and number of the power lines. The increase in distributed generation penetration depth and the presence of multiple distributed generation units in electrical network within a certain local area in close proximity to one another have brought about the concept of the “microgrid” [2].

A microgrid is defined as a localised grouping of electrical and thermal loads with power generators and energy storage. It includes one or more distributed generation units capable to operate with the centralised grid but it can also be operated isolated from the grid while supplying continuous power to various load [3].

The microgrid is responsible for dealing with the requirements of its consumers, providing high power quality and possibly controlling some of the non-critical loads [4]. The key distinction of the microgrid from a conventional power generation is that the power generators are small, they are distributed and located in close proximity to the energy users. Microgrids have various benefits such as improvement of the power quality and reliability of electricity and an increase in the penetration of renewable energy resources to the distribution networks. Due to the close proximity to consumption sites, microgrids are anticipated to provide additional benefits to customers and service providers [5, 6]

Fig. 1.1 shows the conceptual parts of microgrid where various power generators are connected to corresponding loads and a utility grid via power electronic converters.

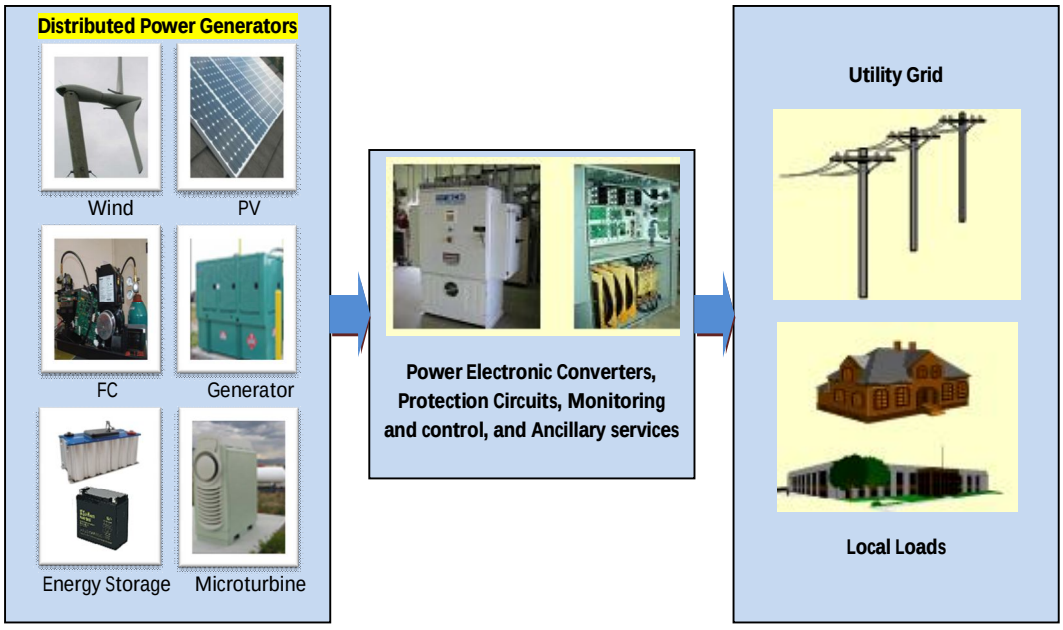


Fig. 1.1 A typical microgrid parts

In the following the configurations of microgrids are introduced together with some of the power generators widely used in microgrids. In addition the major role of the power electronics in the microgrid is shown.

1.2 Microgrid Configurations

Microgrid architectures for integrating renewable energy resources can be classified into AC or DC bus interconnections. A DC microgrid is a system whose different alternative energy sources are connected to a main DC bus-bar through appropriate power electronic interfacing circuits and then the DC bus-bar is connected DC loads. It can also be connected to an AC grid or AC user loads through a DC–AC converter (inverter) which can be bi-directional. An AC microgrid is a system whose different energy sources and loads are interconnected to an AC grid, where necessary through appropriate power electronic circuits.

1.2.1 AC Microgrid Configuration

In the AC microgrid, shown in Fig. 1.2, all the DC and AC sources are connected to the AC utility grid via AC bus-bar. DC sources such as photovoltaic generators and fuel cells are connected to the AC bus through DC–AC inverters and sometimes they also require a DC–DC boost converter as a front-end to step up their low input voltage. In an AC microgrid synchronisation of all AC generators and output of the power converters of the DC sources and energy stores is necessary. Furthermore, due to the non–linear characteristics of power electronics converters, power factor correction and topologies with sophisticated control strategy for harmonic distortion reduction are needed to improve the power quality of the AC bus. Moreover, rapid variations in the output of the renewable sources can lead to excessive voltage and frequency variations of AC bus of an AC microgrid. This can limit the maximum penetration of renewable energy sources into an AC microgrid bus.

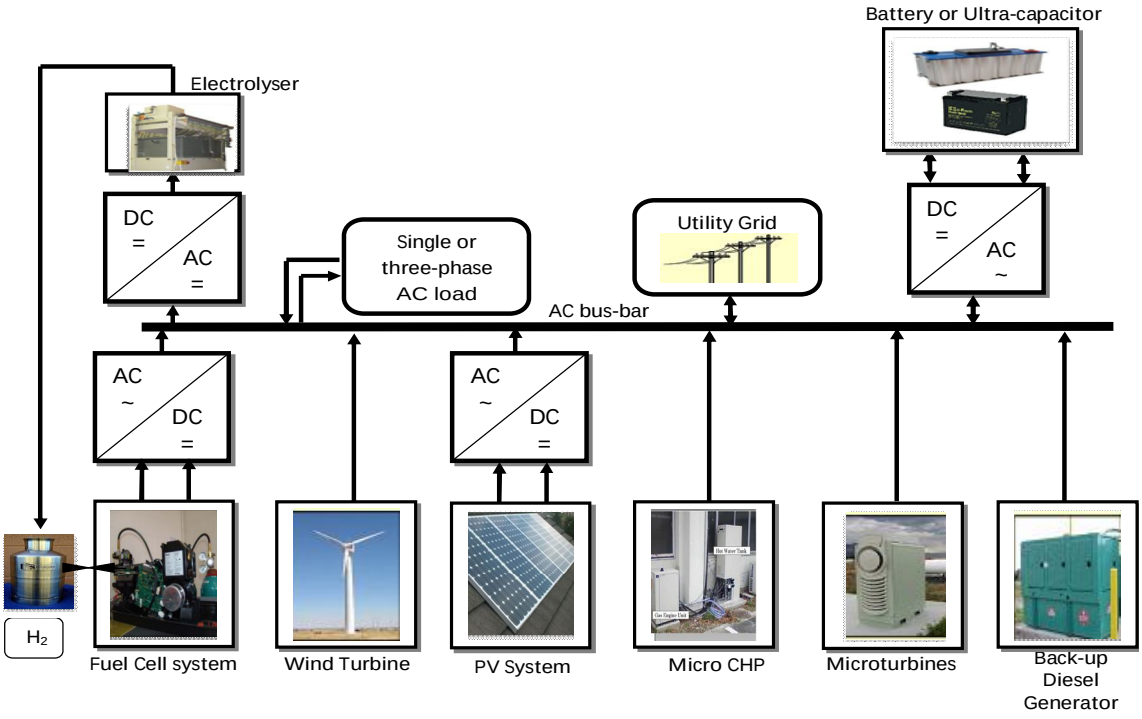


Fig. 1.2 Block diagram of an AC microgrid system

Recently, DC microgrids have show promising features such as improving the grid efficiency and the power quality in addition to increase the penetration of the renewable energy sources to the microgrid bus and elimination of DC–AC power conversion stage required in AC microgrid for the renewable sources and loads. Thus, some negative effect associated with AC microgrid can be avoided.

1.2.2 DC Microgrid Configuration

Fig. 1.3 shows the basic configuration of DC microgrid. As can be seen the DC microgrid may comprise both dispatchable power generators such as a fuel cell, back-up diesel generator or micro (gas) turbines, and non-dispatchable generators, such as solar photovoltaic and wind turbines, and energy storage, in the form of ultracapacitors or batteries. In the DC microgrid configuration, all of the above generators and storage units are connected to the DC bus-bar.

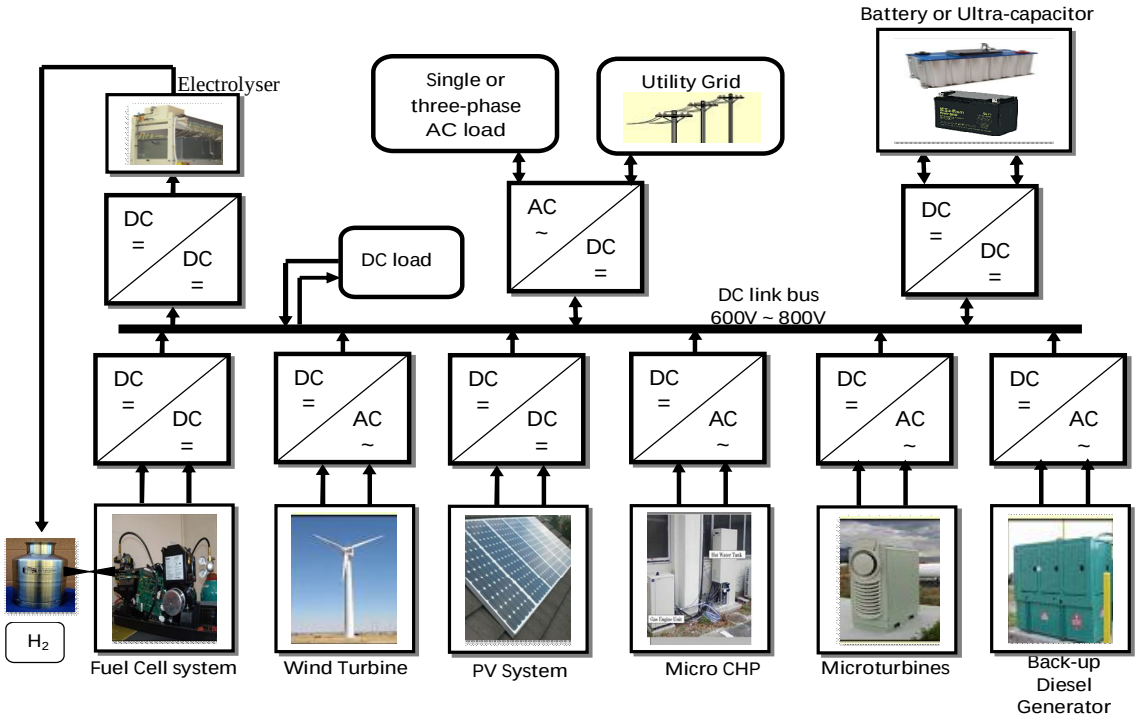


Fig. 1.3 Basic configuration of the DC microgrid system

The AC generators such as the wind turbine, microturbine and back-up diesel generators are connected to the DC bus through an AC–DC converter. For grid-connected operation the power transfers from different generators and storages to the utility grid and AC loads through the main bidirectional DC–AC inverter as shown in Fig. 1.3. The back-up diesel generator and the fuel cell should provide the peak load and charge the short-term storage units simultaneously, while the utility grid through the inverter can maintain the voltage level of the DC bus and cover the required load demand if the DC microgrid fails.

Referring to Fig. 1.3, it can be seen that different configurations of power electronic converters are used to interface these generation resources to a common DC bus-bar. These converters are employed to manage the power flow between the generators, the storage sources and the load and to regulate the DC bus voltage regardless of the voltage variations of their inputs.

The DC microgrid system has the following advantages over the AC microgrid [7-9]:

- Synchronisation of power generators is not needed.
- Unlike AC microgrids, loads connected to the DC bus are not affected by voltage sag and three-phase voltage unbalance and voltage harmonics.
- The power generators and energy storage sources with the DC microgrid are operated cooperatively to control the DC bus voltage and to improve the power quality of the grid.
- Energy storage devices are used in the DC microgrid to compensate power fluctuations caused by the energy sources such as the wind turbine.
- The DC microgrid can supply power to the loads connected with the DC bus when the AC utility line experience abnormal or fault conditions.
- Aside from reducing CO_2 emissions and financial costs, DC microgrids may provide the best solution for increasing the penetration of renewable energy sources in a distribution network, improving the system efficiency and also making plug-and-play grids conceivable.

The disadvantage of this configuration is that the whole microgrid system fails to supply AC power if the DC–AC inverter is out of service. In addition, the multiple power converters required in a DC microgrid may add additional loss to the system operation. Therefore, further research is required to improve the performance and the system efficiency of the converters.

1.3 Microgrid Energy Sources

The key feature of the microgrid is that there should be local electricity generation that matches the load requirements in the microgrid. There are various types of distributed

generation resources that may be considered such as photovoltaic cells, fuel cells, wind turbines, micro combined heat and power (micro-CHP), etc. An overview of some of the clean generation systems is given below.

1.3.1 Photovoltaic

Photovoltaic (PV) cells can convert sunlight directly into electricity using the photovoltaic effect [10]. The cost of PV has declined considerably since the first solar cell was manufactured. A photovoltaic generator consists of a number of modules, formed by the interconnection of photovoltaic cells, connected together in series and parallel to provide the required voltage and current. The output power of PV systems ranges from a few watts for portable applications such as calculators, to megawatt power stations [11]. Photovoltaic arrays integrated in the roofs and facades of buildings are becoming an increasingly common method of power generation within the urban environment. PV is a DC generator source, therefore a DC–AC inverter is required to convert the DC power into AC power at the specified frequency and voltage level and then interfaced with the AC utility grid and loads. For stand-alone or grid connection, PV system can be combined with energy buffer to store the energy in order to be used when the sun is not shining. While PV cells can be effectively used as a source in a microgrids, it they suffers currently from high installation costs and low energy efficiency [9].

1.3.2 Wind Energy Conversion System

A wind energy conversion system (WECS) converts wind energy into electrical energy [1]. Wind as a type of renewable energy has received considerable attention for producing electricity in comparison with other distributed generation resources due to its cost, rapid technological development and the power rating produced by the WECS.

The main component of a WECS is the turbine. This is coupled to the generator either directly (if a multi–pole generator is used) or through a step–up gearbox. The main parts of a wind turbine are the tower, the rotor and the nacelle [1, 9].

Due to the stochastic nature of the wind generators suffer from rapid variations, potentially leading to deviations in the output voltage and frequency, and this limits the penetration of these generators in microgrid [12]. To overcome this problem the wind turbine generators can be incorporated with other power resources such as, back-up diesel generator, energy storage or fuel cells. The energy storage devices such as a battery or ultracapacitor can be used as power assistance for short-term to reduce the intermittency problem of wind generator [13]. But to provide enough energy over time (i.e. for long-term) the integration of PV or fuel cells with wind generator systems appear to be the more efficient and effective solution to the problem of intermittency.

1.3.3 Cogeneration System

Cogeneration or combined heat and power systems (CHP) represent one of the most effective approaches to ensure maximum energy efficiency in microgrid applications since it is produces two kinds of energy, electric power and thermal energy. CHP systems capture the waste heat during the production of electricity and convert it into thermal energy. For small scale private use, such as homes or small commercial buildings, micro-CHP systems can be employed [14]. Most large industrial CHP units generate electricity as the primary product with heat as a secondary output while micro-CHP systems generate heat as the primary product with electricity as a by-product [1, 4]. Thus, energy generation of micro-CHP systems is principally dependent on the heat demand of the consumers. Most micro-CHP systems use natural gas for fuel because it is the cleanest fossil fuel, is widely available, and easily transported through pipelines.

The CHP system can be connected to the DC microgrid through an AC–DC converter (rectifier) as illustrated in Fig. 1.3.

1.3.4 Energy Storage

In practice an energy storage unit is usually considered an essential requirement for a microgrid to allow instantaneous power balancing of distributed generation resources and loads when the microgrid is disconnected from the utility grid (islanding or autonomous) and to ensure uninterrupted supply to priority loads. In addition, the energy storage devices operate in the microgrid system to store surplus energy. The backup energy storage devices that could be included in microgrids are: storage batteries, flywheels, and ultracapacitors. Most of the storage devices such as batteries and ultracapacitors produce a DC voltage, thus a bidirectional DC–AC converter is required for use in an AC microgrid (see Fig. 1.2) while a bidirectional DC–DC converter is utilised to interface them to the DC bus of a DC microgrid (see Fig. 1.3). In contrast, flywheel generators can directly produce AC and hence may feed directly into the AC bus of the AC microgrid [1, 4]. However, a bidirectional AC–DC converter is necessary to interface the flywheel generator to a DC microgrid bus[1].

Some storage devices like ultracapacitors store power at high density but are limited in the amount of energy stored, whereas others like flywheels suffer from low power density but are capable of discharge for a longer time [1].

1.3.5 Fuel Cell Generator

For the future generation of clean electricity, fuel cell (FC) ranks as one of the dominant technologies. Fuel cells are electrochemical devices that convert the chemical energy of

[1] Most of flywheel storage systems use AC–DC–AC conversion stages when connect to AC bus of an AC microgird.

a fuel directly into electrical energy with high efficiency. There are several types of fuel cell, categorised by the type of electrolyte such as proton exchange membrane fuel cell (PEMFC), alkaline fuel cell (AFC), and solid oxide fuel cells (SOFC). Fuel cells have many advantages [9, 13, 15]:

- Fuel cells have the advantage of high power density, and can support the power system for an unlimited time[2].
- They can be used for stationary as well as automotive power generation.
- Fuel cells generated a DC voltage and the only by–products are water and heat.
- Since it is working with zero emissions the fuel cell can be used for indoor operation.
- Moreover, compared to the PV and wind energy the fuel cells can continuously producing power if the fuel is available.

Despite these advantages, the cost of fuel cell is relatively high[3] in comparison with conventional power generators. In addition fuel cells have a limited lifetime and require a special treatment for the fuel production[4].

However, the major problem of the fuel cell is that it has a relatively slow dynamic response to sudden load changes because of the slow internal electrochemical reactions and the processing time required for the ancillary equipments such as valve, pumps, and a hydrogen reformer. Therefore, in order to supply electric power to transient loads the fuel cell requires an energy storage system, such as batteries or ultracapacitors, to fill the gap between the output power delivered by the fuel cell and the power required by

[2]In a microgrid system storage devices can provide only for short-term power requirements, while fuel cells and back-up diesel generator can supply the long-term power demand.
[3]This is due to the very high costs of the catalysts, membrane materials, and fabrication processes for collector plate.
[4] Pure hydrogen gas as the main fuel is necessary for some types of fuel cell such as PEMFC.

the load. In addition, energy storage can help to improve the fuel cell performance (see next Chapter for further details).

1.4 Power Electronic Interface Circuit for a Microgrid

One of most important features of a microgrid is the advanced structure which can facilitate the connections of various AC and DC renewable energy resources, energy storage devices, utility grid and different AC and DC loads with optimal operation and high efficiency. To achieve those goals, power electronics converters plays a very important role in order to interface different sources and loads to a microgrid. Power electronic converters are utilised in microgrids to manage the flow of power and convert it into suitable DC or AC form as required. A number of converter configurations, such as AC–DC rectifiers, DC–DC converters, and DC–AC inverters, are necessary to achieve the many functions within a microgrid, as shown in Fig. 1.2 and Fig. 1.3.

However, power electronic circuits are quite costly due to their complicated technology, they may increase the losses through the microgrid system, and they are the most common sources of harmonics and low power quality for a microgrid bus and resources. Reference [16] describes a new passive AC–DC diode rectifier circuit with step–up voltage properties, developed by the author, that can be employed as a front-end converter for connecting an AC generator to a DC microgrid. It can also be used to maintain the power quality on the AC bus of an AC microgrid system.

Furthermore, reliability and functionality for the selectable power electronics topology is needed [17]. Reliability will allow long term commercial penetration of renewable energy sources using power electronics whilst functionality will expand the exploitation of microgrid and improve power quality.

1.5 Objectives of the Thesis

The aim of this study is to investigate and develop high-efficiency power electronic converters for the interconnection of elements of a DC microgrid. The main focus is on the power electronic converter topologies for connecting fuel cells and ultracapacitors to a DC microgrid for stationary power distribution systems. The objectives of this research can be divided into the following parts:

- To investigate existing unidirectional and bidirectional DC–DC converter topologies that are suited for the fuel cell and the ultracapacitor energy buffer.
- To develop a new converter topology, optimised for operation with a fuel cell.
- To study the dynamic performance of the fuel cell and the associated power electronics converter to select an appropriate controller design for the developed fuel cell converter.
- To digitally implement and test the proposed fuel cell converter system.
- To develop a dynamic model describing the behaviour of the ultracapacitor that can then be interfaced with a model of the power electronics converter.
- To improve the performance of the ultracapacitor converter by means of a novel modulation scheme to achieve optimum performance.

1.6 Outline of the Thesis

The structure of the thesis is organised as follows:

In Chapter 2, the characteristics of the fuel cell and the ultracapacitor are described and studied. Experiments have been conducted on a fuel cell to establish the steady-state and the dynamic performance of this source. A model of an ultracapacitor is established

in Matlab. A number of fuel cell–ultracapacitor DC microgrid configurations are presented. The advantages, disadvantages, and features of several unidirectional and bidirectional DC–DC converter topologies for the fuel cell and ultracapacitor applications are discussed. Based on the electrical output characteristics of the fuel cell and the ultracapacitor, appropriate power electronic converter topologies are selected to interface the fuel cell and the ultracapacitor to the DC bus of a DC microgrid.

Chapter 3 presents a detailed steady-state analysis of a new fuel cell converter. Means to improve the converter efficiency are described. A comparison of the proposed converter with other competing fuel cell converter topologies is presented. Experimental results are reported and compared with the results of detailed simulation.

In Chapter 4, a full dynamic model for the fuel cell converter based on the state–space averaging method is derived. The converter dynamic performance is evaluated and compared with that of other configurations using the developed dynamic model. Based on the validated dynamic model a two–loop digital control system for the fuel cell power converter has been designed. Three different approaches have been used to demonstrate the fidelity and effectiveness of the dynamic modelling. The developed controller system has been executed and validated using real processor hardware.

Chapter 5 provides a comparative study of various modulation schemes that can be used to control the power flow of the ultracapacitor bidirectional DC–DC converter.

Chapter 6 details a new optimal modulation scheme to control the power flow of the bidirectional converter is presented, based on a comprehensive mathematical analysis. Theoretical analyses are verified using the detailed simulation results.

Finally, Chapter 7 presents the conclusions on this study and suggestions for future work.

Chapter Two

Fuel Cell–Ultracapacitor DC Microgrid System

2.1 Introduction

As shown in the previous Chapter, a DC microgrid is composed of different dispatchable and non-dispatchable power generators and energy buffers, such as FCs and ultracapacitors, which are employed to provide the steady-state and transient power demanded by the load. To interface these generation resources to a common DC bus-bar, different configurations of power electronic converters have been proposed in the literature. For the FC, a unidirectional DC–DC converter is utilised, for the ultracapacitor, however, a bidirectional DC–DC converter is needed to maintain the state-of-the-charge (SOC) of the ultracapacitor. The overall efficiency of the microgrid will depend on the efficiency of these converters. High efficiency and low cost converters are very important to obtain a cost-effective solution. In addition, the power electronics converters must be chosen in respect to the characteristics of these generation resources.

This Chapter introduces an overview on different of DC–DC converter topologies and investigates their applicability for FC and ultracapacitor electricity generators based on the electrical output characteristics of these resources. The FC and ultracapacitor characteristics and properties are also introduced in this Chapter. A number of configurations that can be employed to interface the ultracapacitor with the FC generator forming part of a DC bus microgrid are presented.

2.2 FC Power Generator

Fuel cells are static electrochemical devices, which convert the chemical energy of fuel into electrical energy [15]. One of the most popular types of FC for low temperature operation (below or around 200^{o}C) that uses hydrogen as a fuel is the proton exchange membrane fuel cell (PEMFC). The PEMFC can be used for stationary as well as automotive power generation. The output power characteristics of the PEMFC are determined by the kinetics of the electrochemical reactions, internal electrical and ionic resistances and the crossover of reactants [18].

In this section, the principle of operation, the voltage-current characteristics of the PEMFC, the effect of current ripple and PEMFC dynamic performance are presented. These characteristics and properties must be considered while selecting the FC power converter (see Section 2.5).

2.2.1 Principle of Operation

Fig. 2.1 illustrates the FC reaction for the PEMFC type. The hydrogen passes over the anode and with assistance of a catalyst the H_2 gas separates into electrons e^- and hydrogen proton ions H^+. The electrons cannot pass through the membrane and are forced to flow through an external circuit, consequently creating electricity, while positive ions can pass through the membrane and recombine with oxygen O_2 which flows through the cathode; the product of this recombination is pure water H_2O [15, 18]. The chemical FC reaction process is given below [19]:

$$H_2 + \frac{1}{2}O_2 \longrightarrow H_2O + \text{heat} + \text{electricity} \tag{2.1}$$

The voltage produced by a single cell is usually less than 1.2 volt. For utility application multiple cells are bundled together in series to form a FC stack. The stack voltage is the

number of cells times the average voltage of the one cell. Fig. 2.2 shows the structure of the PEMFC stack [13].

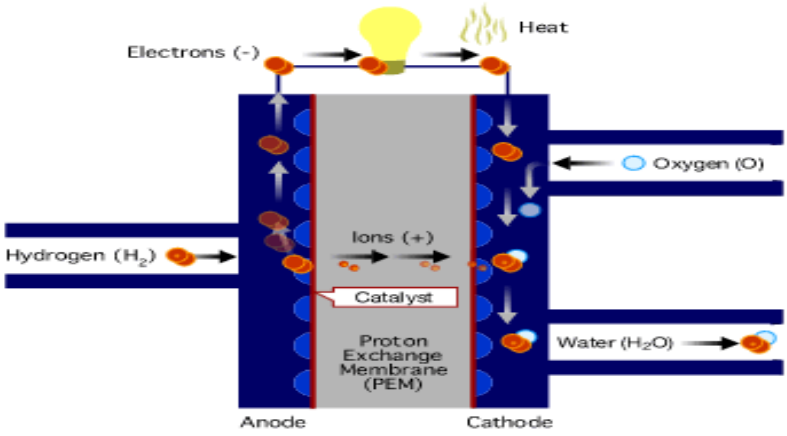


Fig. 2.1 PEM fuel cell operation [20]

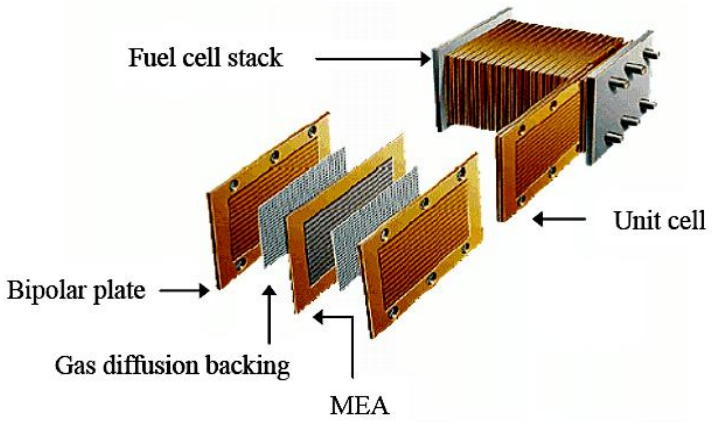


Fig. 2.2 PEMFC stack structure; MEA is a Membrane Electrode Assemblies [13]

2.2.2 Voltage-Current Characteristics of FC

FC operation is similar to that of a battery in that a FC uses an anode and a cathode and the output is a DC[1] voltage. But the output voltage of the FC exhibit significant degree of regulation with increasing current. Fig. 2.3 shows a typical voltage-current characteristic of a single cell. It can be seen that the cell voltage drops with current

[1] However, the anode and cathode of the battery are metal/fluids while for a FC are gasses

density increase. This is due to three losses which are known as activation losses, ohmic losses, and concentration losses [21].

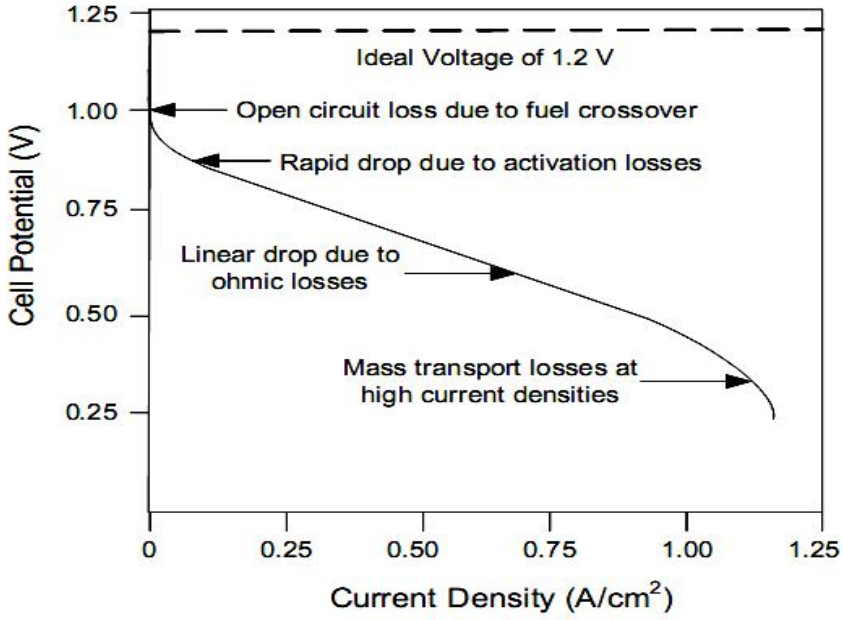


Fig. 2.3 Voltage-current Characteristic of FC [22]

Activation losses are caused by the slowness of the chemical reactions taking place on the surface of the electrodes [22]. The ohmic loss is due to the resistance of the membrane, electrodes material, and the various interconnections. Operation of FC in the ohmic loss region is recommended since the voltage drop is proportional with the current density. In this region the FC can be represented as a Thevenin equivalent circuit consisting of a constant DC voltage source (V_{fc_o}) with a series resistance (R_{fc}), as shown in Fig. 2.4.

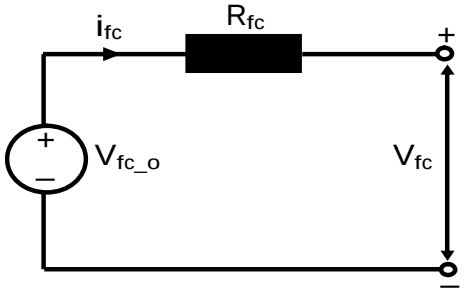


Fig. 2.4 Simplified FC equivalent circuit model

The ohmic resistance depends on the membrane characteristic and given as [18]:

$$R_{fc} = \int_0^{L_m} \frac{dx}{A_m \gamma_T} \tag{2.2}$$

where L_m is the thickness of membrane, A_m is the effective area of membrane, and γ is the conductivity of the membrane at the operation of temperature.

During the reaction process at high current density the change in the concentration of reactants results in mass transportation losses (or concentration losses), leading to a rapid drop in the voltage, as indicated in Fig. 2.3. Prolonged operation in this region leads to damage to the FC and has a very low efficiency [9]. The voltage drops due to the activation and concentration losses can be represented by the equivalent resistances R_{act} and R_{con}. Hence, the actual cell voltage V_{fc} is:

$$V_{fc} = \Delta V_{ohmic} - \Delta V_{conc} - \Delta V_{activ} \tag{2.3}$$

where ΔV_{ohmic} , ΔV_{conc} , and ΔV_{activ} are the voltage drop due to ohmic, concentration, and activation losses respectively.

As described in Section 2.2.1, the two electrodes of the PEMFC are separated by a membrane (see Fig. 2.1) which prevents the flow of electrons and only passes positive ions. The electrons flow from anode through the external circuit and recombine with the positive ions H^+ at the surface of the cathode. Hence, charged layers of opposite polarity are formed at the cathode and the electrolyte side of the membrane. Therefore, the cathode–membrane interface acts like a very large capacitor[2], which is a store of electrical charge and energy [18, 23]. This is called the "double-layer" effect. A FC

[2] The PEMFC uses porous carbon electrodes; the extremely small pores measured in nanometres in such carbons give the material a very large active internal surface, thus the capacitance C_{dl} is very large and can be in the order of several Farads.

dynamic model considering this effect is given in Fig. 2.5 as a first-order equivalent circuit [9, 24], where C_{dl} is the equivalent capacitance of double-layer.

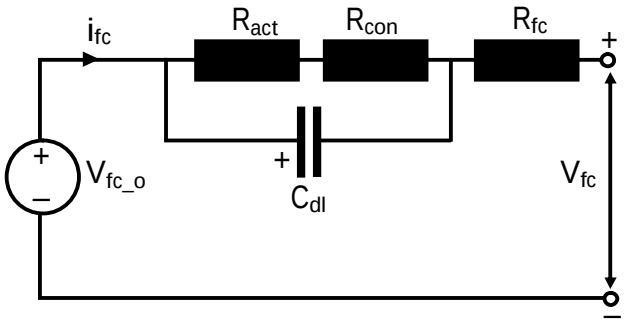


Fig. 2.5 First-order FC equivalent circuit model

2.2.3 Constraints on FC Current

The FC is sensitive to any current ripple since it decreases the service life of the stack and impacts on the diffusion layer of the FC stack [25]. Moreover, at high ripple the FC operation could deviate from the ohmic region to the concentration region resulting in a possible shut down of the FC system. In addition to the ripple current, reverse current of the FC operation should be avoided and the load current should be limited to less than the maximum allowable current.

Therefore, it is preferable to employ a power conditioning unit that can avoid all the negative effects without adding protection circuits.

2.2.4 Dynamic Performance of the Ballard FC System

As the FC is the dispatchable generator in the system its dynamic response to load changes is vital to the design of the control system. Therefore, in this section experiments are described that have been carried out to establish of the steady-state and the dynamic performance of the Ballard Nexa^{TM} 1.2kW PEMFC system. The results

have been used to upgrade an existing Matlab/Simulink model for later use with the whole FC converter model which is described in Chapter 4 (see Fig. 4.17).

2.2.4.1 Nexa FC Power Module Specifications

The Ballard Nexa FC is produced by Ballard Power Systems as an educational unit, and one such unit installed in the Projects Laboratory of the Electrical Power Group. It uses Ballard PEM technology and it is very suited for a diversity of power engineering purposes such as portable power source, back-up power generator, and stationary power supply system. It is able to produce 1.2 kW at a rated output voltage of 26 DC volts while the no-load voltage is 43V. The cell voltage is 0.6V at full load and 1V at light load. The rated gross current (which includes ancillary loads such as control board, pump, and cooling fan) that the module can produce is 46A and the maximum current is 60A. The ancillary loads consume 35 W at no-load and 250 W at full load [26]. Table 2.1 shows the major specifications of the Nexa Power Module.

TABLE 2.1
MAIN SPECIFICATIONS OF THE BALLARD NEXA FC POWER MODULE

Start-up process of the system	10-30s from cold starting to running state
H_2 pressure ranging	0.7-17.2 bar
Composition for H_2	99.99%
Composition for O_2	21% (from air supply)
The maximum acceptable peak-peak ripple current	35% at rated current
Ambient temperature	3.3^0C-30^0C
FC efficiency	38% at full load and 50% at light load
Maximum fuel consumption	18.5 Standard Litres per minute (slpm)
Air flow consumption	less than 90slpm at rated power

In addition, this system requires an external 5V DC power supply during start-up and its protection circuit shuts it down if the stack voltage is less than 18V.

2.2.4.2 Experimental Set-up

Since the exact dynamic response of the FC is important to select a proper controller design (see Section 4.4) for the proposed FC converter (see Chapter 3), an experiment was set up on the Nexa Power Module as shown in the block diagram of Fig. 2.6.

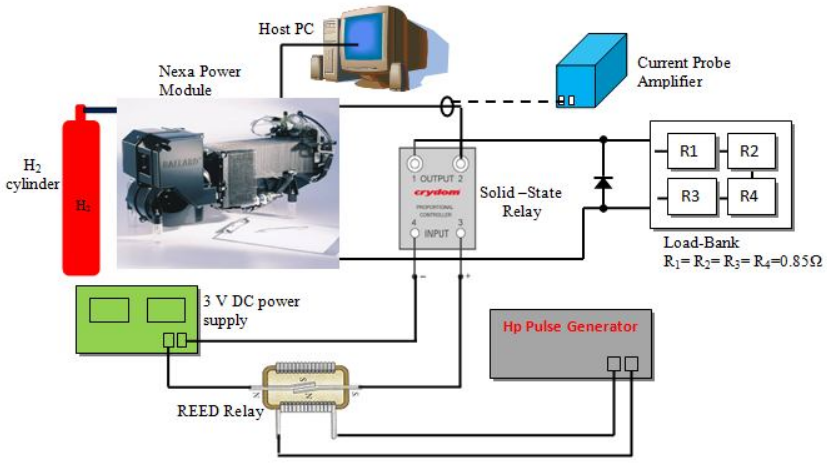


Fig. 2.6 The experimental set-up to evaluate the accurate dynamic response of the Nexa Power FC Module

Initially, the experimental set-up was composed of the Nexa Power Module system, a low-inductance resistive load bank with four 0.85 Ω sections, a mechanical relay which was included with the Ballard system, and auxiliary equipment. The Ballard Nexa FC is equipped with a control board that transmits data via a communication serial port to a host PC for recording and displaying internal and external variables [26]. Using the "Nexamon OEM"[3] data log file the transient response characteristic of the Nexa system was obtained as shown in Fig. 2.7. These results show that the FC can respond to load changes from no-load to the full-load in 0.5 second. In the no-load state it was observed on the "Nexamon OEM Screen" that the FC voltage is 42V and a small current is drawn from the FC stack, about 1A, that is due to the ancillary loads.

[3] Nexamon OEM is software programs to record and display different internal and external variables such as, stack voltage, stack current, fuel pressure, fuel consumption, stack power ….etc.

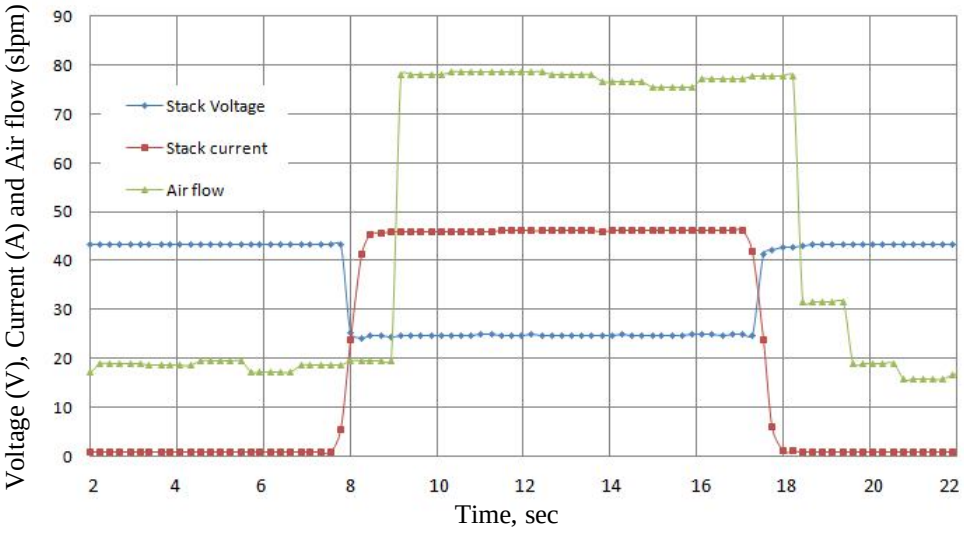


Fig. 2.7 Measured transient response of Nexa FC Power Module using "Nexamon OEM" data log file

While adequate for general analysis the update time (0.2sec) of this data acquisition system is inadequate for measuring the transient response of the FC stack accurately. Therefore, an experiment was set up using fast-acting switches (Crydom D06D MOSFET solid-state relay) and high speed transducers (TM503 transducer) as shown in Fig. 2.6 to extract the exact dynamic response. A solid-state relay is used to independently change the resistive load across the FC output. The ON-OFF state of the Crydom relay is controlled using a HP pulse function generator (set on 71.42 mHz)[4]. The generated pulses are applied to the coil of a Reed Relay. The control terminals of the solid-state relay are connected to the output of a Reed Relay and the output of a 3V power supply. Three resistor sections were used, with two sections connected in series and paralleled with the third section, thus applying 0.57Ω across the FC to draw the nominal current of 46A.

Fig. 2.8 shows that when full–load is applied from no-load the gross stack current initially increases to about 1.3 times the nominal current (46A) before settling to the

[4] The main feature of this function generator that provides very low frequency signals.

rated value in about 0.24 second. In comparison, the recorded response in the FC "Nexamon OEM" data log files (Fig. 2.7) doesn't show this current spike.

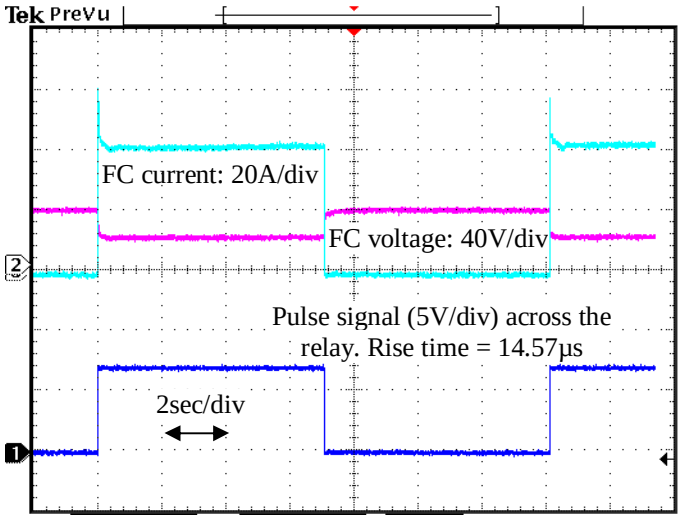


Fig. 2.8 Accurate transient response using experimental set-up in Fig. 2.6

The current peak is the result of charge double-layers on the electrodes of the cell. Depending on the density of the charges, electrons, and ions on the electrode and electrolyte surfaces a higher peak current can be generated.

Further details of dynamic response of the Nexa FC are shown in Fig. 2.9.

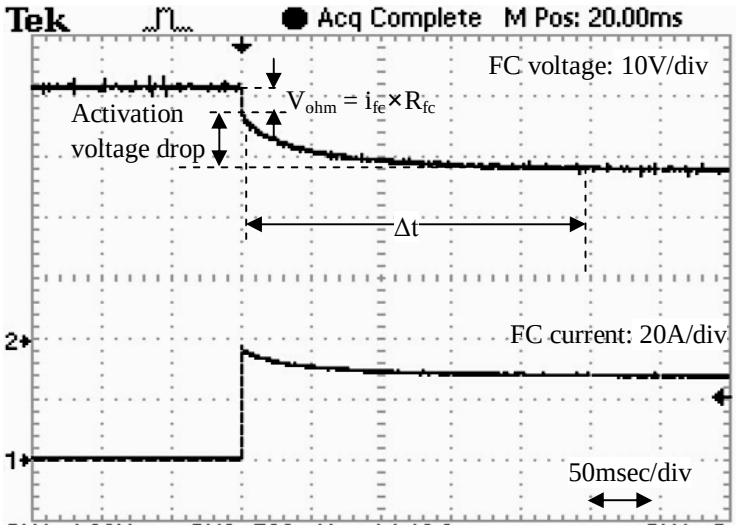
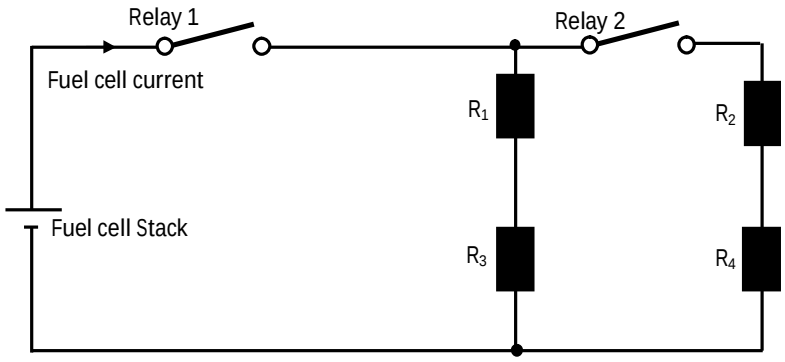


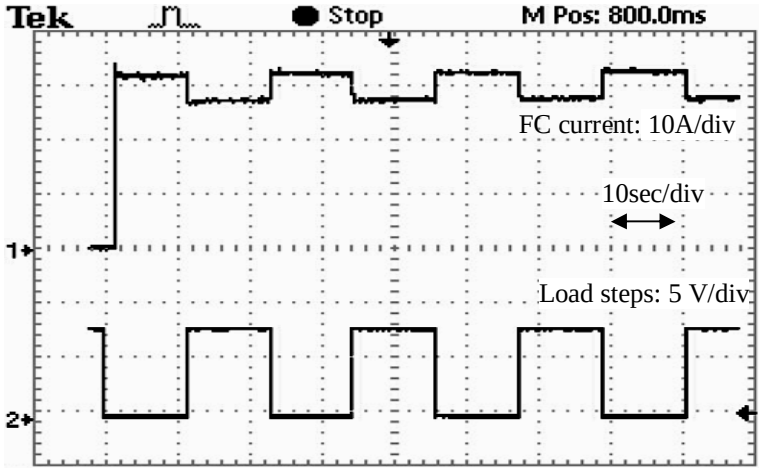
Fig. 2.9 Dynamic Response of the FC shows the effect of the double–layer capacitor C_{dl}

It can be seen that when the load current steps up from 0A to 40A the FC output voltage shows an instantaneous change from 42V to 38V due to the ohmic resistance R_{fc}, but then decays further to the steady-state value (28V) after $\Delta t = 0.24s$. The latter is due to the activation losses, caused by fuel starvation [27].

It may be thought that the response in Fig. 2.8 and Fig. 2.9 demonstrate the ability of the PEMFC to follow rapid load variations. However, further tests at part–load, as described below, have shown that the double–layer effect is restricted to load changes from no–load after a sufficiently long period to re-establish the doubler–layer.



(a)



(b)

Fig. 2.10 Experiment set-up to evaluate the FC operation for different load demands: (a) equivalent circuit diagram and (b) measured FC current results

Using the test set–up in Fig. 2.10a the response of the FC to small variations in load demand while delivering a substantial proportion of the nominal current was investigated. Initially, when applying 70% load from no–load, the current peak present, but at subsequent cycling of the load by 10% the peaks are absent (Fig. 2.10b).

Due to the chemical reaction inside the FC stack, it is clear that the FC needs time to recover to the steady-state voltage when the load changes. The FC cannot keep the output voltage constant. Hence, a power conditioning unit, such as DC-DC converter, is necessary to obtain a constant voltage. To improve the dynamic response of the FC, avoid the fuel starvation problem, maintain constant output power for the FC, and absorb the surplus energy during transient load drops, an ultracapacitor energy buffer is needed (see Section 2.4.2 for more detail about the FC-UC interaction).

2.2.4.3 Dynamic Model of the PEMFC

The dynamic model of PEMFC used in this study is based on an existing Matlab model with added flow rate regulators to control the fuel and air utilization (see Appendix A). The load conditions of the experiment were applied to the FC model as illustrated in Appendix A and by comparing the responses to load changes the unknown parameters for the real FC were obtained. As indicated in Appendix A, the Simulink results show that the modelling matches well with the experimental set-up. This model has been integrated with the PSpice model of the FC converter (see Chapter 3) using the SLPS simulator to develop the FC control system and algorithms, as will be described in Chapter 4.

2.3 Ultracapacitor Energy Buffer

Ultracapacitors (UCs) or Supercapacitors, also called "electric double layer" capacitors, are electrochemical capacitors with very high capacitance values[5] and very large energy density compared to the conventional capacitors. The same basic principle of conventional capacitors applies to ultracapacitors, but with UCs the electrodes have a much larger surface area and thinner dielectrics to achieve larger capacitances [13, 28]. Compared with batteries, UCs have a longer lifetime[6] and higher power density. However, UCs have lower energy density than batteries, which in most cases determines the viability of their employment in a particular high power application. As indicated in Chapter 1, storage devices are introduced in microgrids in order to secure their power quality, power regulation and to offer ancillary services during transient periods.

This section briefly describes the operational principle and the electrical characteristic of the UC energy buffer. This section also introduces a developed equivalent circuit model for an UC that takes into account the most important UC characteristic, such as the non-linear voltage-capacitance dependency.

2.3.1 Principle of Operation

An ultracapacitor comprises two electrodes, a separator, and an electrolyte, as depicted in Fig. 2.11. In an UC, energy is stored by the separation of positive and negative charges at the interfaces between the electrode and the electrolyte. This is called the double–layer capacitor phenomenon [29, 30].

[5] For the Maxwell Boostcap™ technology capacitance values reaching up to 3000 Farads for a single cell with voltage rating up to 2.7V.
[6] Compared to the batteries, the UCs have a considerably longer cycle life because there are no chemical reactions during charging and discharging.

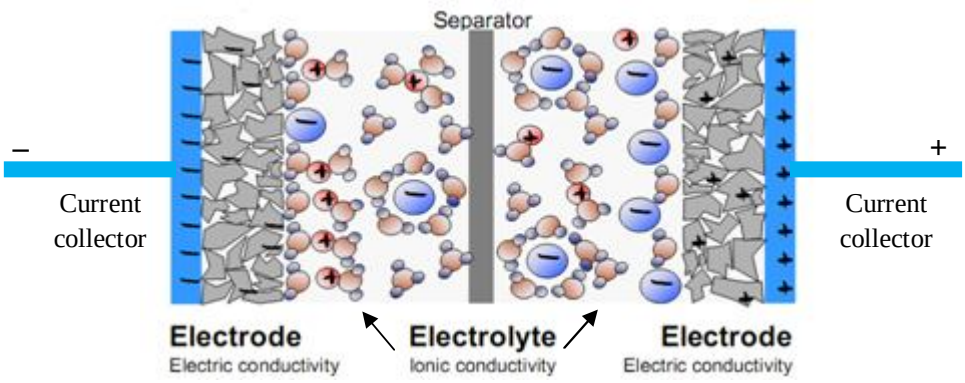


Fig. 2.11 Principle of operation of Ultracapacitor [29]

Three main factors determine the amount of energy that can be stored in an UC: the separation distance between the electrodes, the surface area of electrode, and insulating layers which are separating the electrodes [31]. The two electrodes consist of a porous nanostructure made of carbon materials to provide a larger surface area than conventional capacitors. To interface the electrodes with the terminal connection of the UC, current collectors with a high conductivity are employed. The electrodes (or the anode and cathode) are separated by a thin isolation separator which allows the ions to move freely and blocks the electrons [32]. The voltage rating for a single cell of the UC is determined by the electrolyte properties. Most types of electrolyte, such as organic electrolytes, generally give a rated voltage less than 3V for a single UC cell. This voltage level is very low and therefore UC cells are connected in series to achieve a higher voltage level by forming what is known as a UC module. However, this of course increases the equivalent series resistance (ESR) of the UC (for the BMOD0165 module the ESR is about 6.3mΩ) and therefore it is desirable that the ions have high mobility in the electrolyte to reduce the ESR of the UC module [33]. Due to the cell's leakage current there is the possibility of an imbalance in the distribution of voltages across the UC cells [13]. Therefore, active or passive balance circuits are essential to protect each cell from overvoltage.

2.3.2 Electrical Characteristic of Ultracapacitor

The performance of an UC can be characterised by its terminal voltage during discharging and charging at different current rates. Unlike batteries, the parameters of the UCs depend on the voltage, rather than the current, since the charge stored is based on the capacitance and the voltage. An UC's voltage profile has capacitive and resistive components. The capacitive component indicates the charge or discharge energy within the UC. The resistive component represents the voltage drop due to the internal ESR of the UC [13]. The voltage profile of the UC during constant current discharge is illustrated in Fig. 2.12.

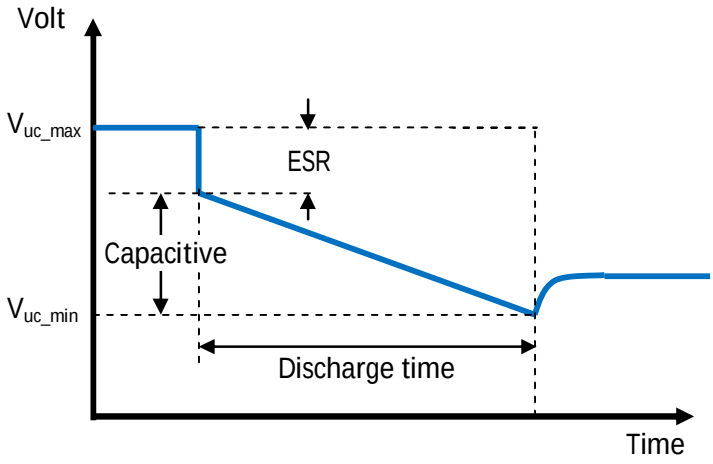


Fig. 2.12 Constant current discharge profile of the UC

Compared to the batteries, UCs can deliver 10–20 times more power and they can be discharged and charged very fast [30]. This is very important feature in order to match the slower power output of the FC and provide the required power for the DC load or AC grid to improve the performance characteristics of the FC-UC DC microgrid. However, this feature will only be of use if the DC-DC converter has been selected appropriately.

2.3.3 Dynamic Modelling of the Maxwell Ultracapacitor

In order to evaluate the UC system performance, it is necessary to develop a dynamic model describing the behaviour of the UC that can then be integrated with a model of the power electronics converter. A number of UC models have been proposed in the literature [34-38]. The UC can be modelled as an ideal capacitor C in series with a resistor R_{esr}, as shown in Fig. 2.13a . However, this is a simplified model for the UC and it is not appropriate if a fast transient response is sought. A first-order model for an UC including the self-discharge effect[7] is shown in Fig. 2.13b [37]. It consists of three components, which include a voltage–independent capacitance C, an equivalent series resistance R_{esr}, and a self-discharge resistance R_p which models the self-discharge effect [38].

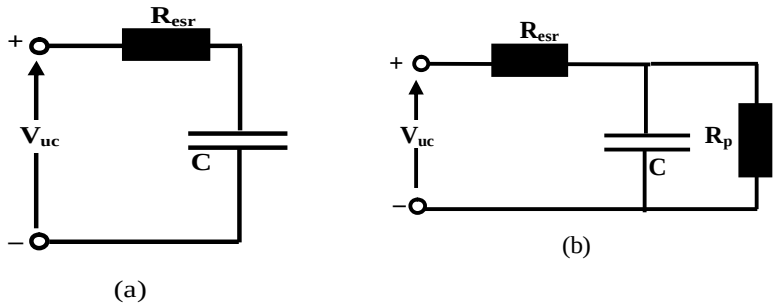


Fig. 2.13 Different equivalent circuit models for the UC: (a) RC model (b) first-order dynamic model [37]

It can be observed from Fig. 2.13 a and b that unlike the FC equivalent circuit, the UC model is a purely passive model, with no voltage or current sources.

The above UC equivalent models assume a linear behaviour for the UC. However, the UC exhibits a non-linear voltage characteristic and its dynamics are related to the temperature, the frequency of the current and the voltage across the capacitance [35].

[7] The electrolyte between the electrodes passes a small amount of leakage current which causes the voltage of a charged UC to decay over time. This phenomenon is known as the self-discharge effect.

Therefore, more accurate model consider the non-linearity behaviour of the UC was proposed in [39]. Based on that model, an equivalent circuit model of UC energy buffer is introduced in this section that models the non-linear voltage-capacitance dependency of the UC using Matlab/Simulink. Fig. 2.14 shows the modified equivalent UC circuit model.

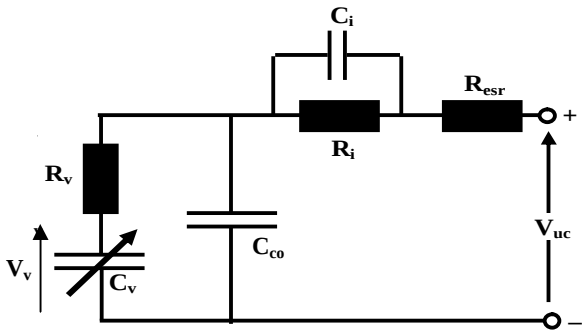


Fig. 2.14 Equivalent circuit used to model the Maxwell BMOD0165 ultracapacitor

As can be seen this equivalent circuit consists of 6 components: C_v is the voltage–dependant capacitance[8], C_{co} is a constant capacitance, R_v is the ESR DC resistance, R_i represents the ionic resistance in the electrolyte, and C_i represents the capacitance utilised to cancel the effect of R_i at high frequencies.

To take into account the capacitance variation in respect to the voltage, the main capacitance C for the UC is represented as the sum of a constant capacitance C_{co} and non-linear capacitance $C_v = K_v V_v$, so that the total capacitance given as

$$C = C_v + C_{co} \tag{2.4}$$

where K_v is a non–linear function of V_v

The voltage-capacitance data was extracted from the test cycle curve for a Maxwell BMOD0165 ultracapacitor as provided by the manufacturer [29, 40, 41], and is used in

[8] The capacitance-voltage dependency is due to reduction in the distance separating the charges at the cathode–separator interface with an increase in voltage, leading to an increase in capacitance as a consequence.

the proposed model as shown in Table 2.2. The obtained voltage-capacitance relationship is depicted in Fig. 2.15.

TABLE 2.2
MAIN SPECIFICATIONS OF THE MAXWELL BOOSTCAPTM UC MODULE

Nominal Capacitance C	165 F
Rated Voltage V_{uc}	48V
Max continuous Current I_{uc_max}	98 A
Leakage current	5.2 mA
Operating Temperature range	-40^0C to $+65^0$C
Energy Available E_{uc}	54 Wh
Number of cell N_{uc}	18
Capacitance of each cell C_{uc}	3000 F
Constant Capacitance $C_{co} = (2/3)\times C$	110F
ESR, DC R_v	6.3 mΩ
ESR, AC	5.2 mΩ
$C_i = C_{co}$	110 F

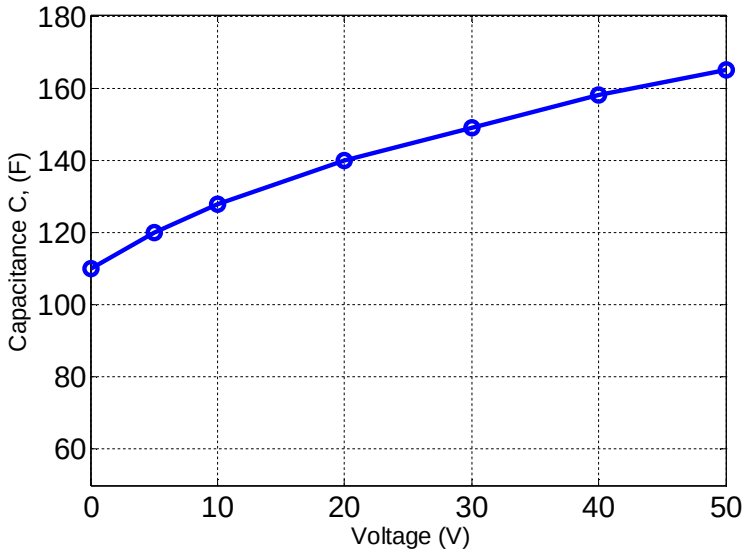
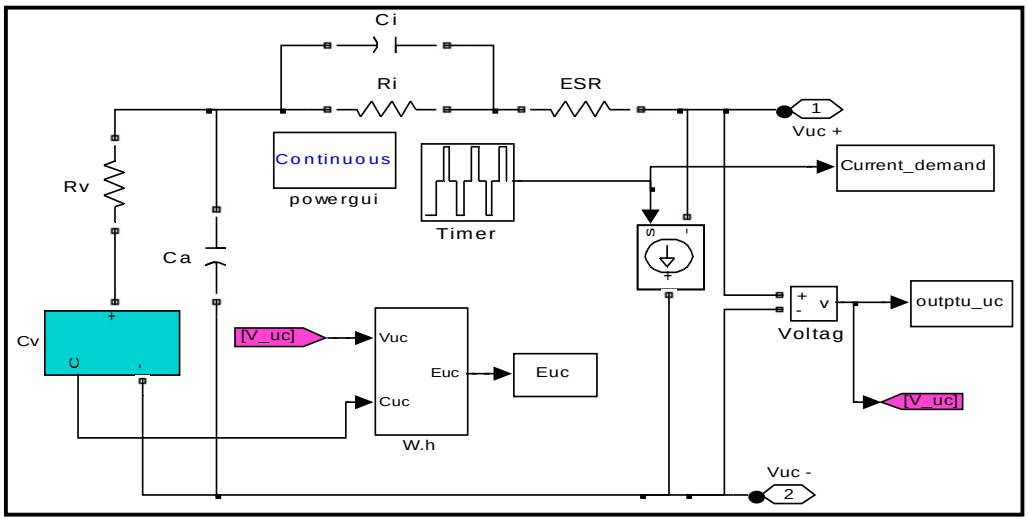
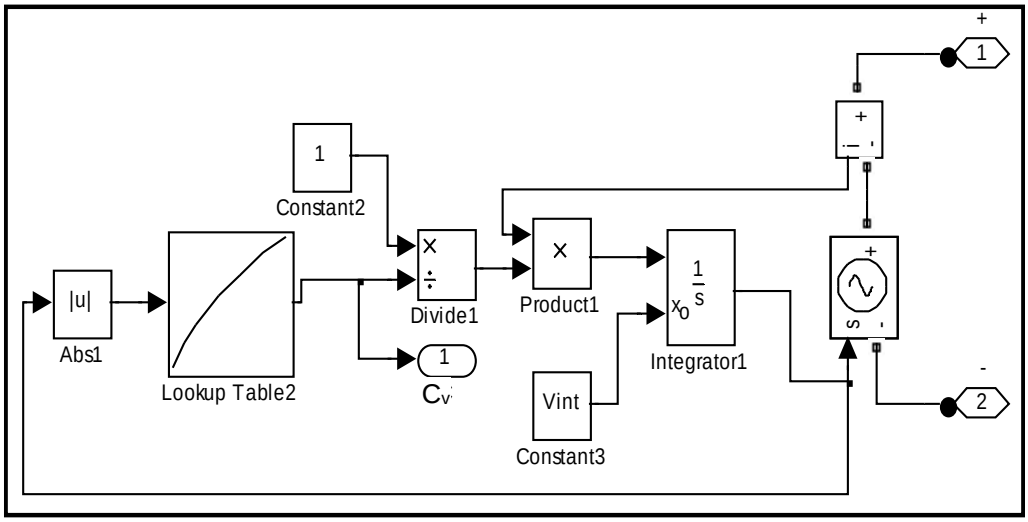


Fig. 2.15 UC capacitance as a function of the voltage

The equivalent circuit has been modelled in Matlab/Simulink as shown in Fig. 2.16a.



(a)



(b)

Fig. 2.16 Simulink block diagrams of (a) the UC model , (b) the details of block C_v, which is represent the non-linear capacitance

Fig. 2.16b shows the Simulink block diagram which is used to represent the non-linear voltage-dependency of the capacitance for the UC. Fig. 2.17 illustrates the simulation results which is represents the voltage behaviour of the UC in the time range of seconds in response to charge or discharge action at constant current (in order of 20A). Measured results in [40] and modelled voltage characteristics are compared which show that the proposed model very closely matches the measured results of BMOD0165 ultracapacitor.

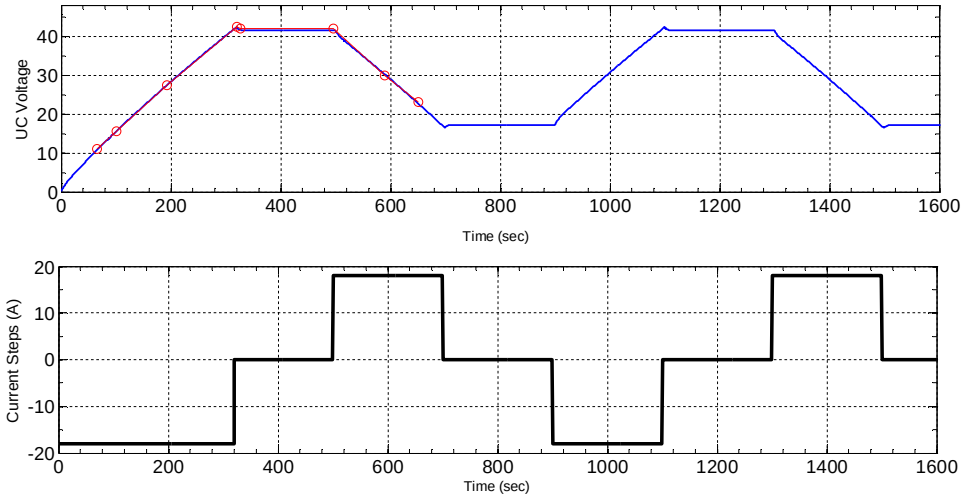


Fig. 2.17 Measured (red) and modelled (blue) results show the voltage characteristic of the UC based on the Maxwell 6-step evaluation test (black) at 20A

Fig. 2.18 show the modelled charge characteristics of the Maxwell BMOD0165 UC at different charge current values. It can be seen that the voltage increases non-linearly with charge time. At a large charge current, the rated voltage increase is much higher than at a small current value.

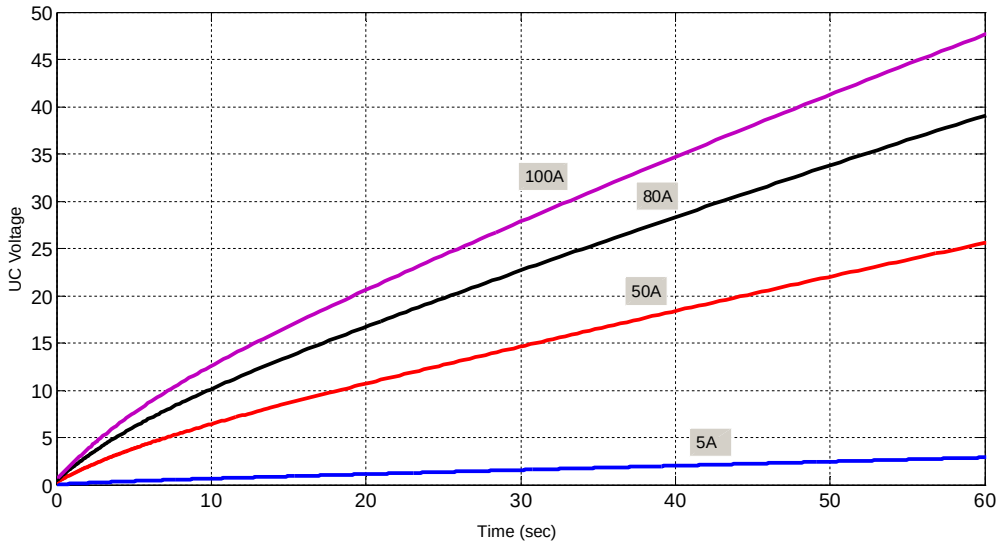


Fig. 2.18 Simulation results of the modelled charge characteristics for the Maxwell BMOD0165 UC

In Chapter 6 the Simulink model is interfaced with the model of an isolated bidirectional DC–DC converter, simulated in PSpice via the SLPS interface, to achieve an accurate dynamic performance for the whole UC converter model.

2.4 Configurations of Fuel Cell–Ultracapacitor DC Microgrid

2.4.1 Overview of Configurations

To compensate for the sluggish response of the FC in supplying the amount of power demanded by the load, a fast response energy buffer such as ultracapacitor is needed. Several configurations have been proposed to interface the ultracapacitor to the FC system. As indicated in Chapter one, to simplify the design of the DC–AC converter of DC microgrid a DC link voltage between 600 and 800V is required. Fig. 2.19 shows different configurations of the fuel cell–ultracapacitor (FC–UC) DC microgrid.

In the first configuration, shown in Fig. 2.19a, the FC and the UC are connected directly in parallel to the DC link forming a passive FC–UC hybrid connection [42, 43]. With this configuration no converters are employed for the FC or the UC. Hence, low losses and low cost can be achieved. The main problem associated with this configuration is that no direct control is included for the FC current and UC charging/discharging and the UC energy cannot be fully used. In addition, the impedance mismatches between the parts of this configuration lead to starvation problem and heavy mechanical stresses on the FC system [18, 44]. To control the current of the FC, an active FC–UC hybrid configuration based on connecting a unidirectional DC-DC converter between the FC and the DC link is illustrated in Fig. 2.19b [27]. With this configuration a rapid rise of the FC current is avoided and thus prevents the fuel starvation. In contrast to the first configuration in Fig. 2.19a, a low–voltage FC source can be utilised. However, since the UC is connected directly to the DC link it must have a high voltage rating. Also, the

power between the UC and the DC link is uncontrolled, therefore this configuration is not a good solution for power management between the FC, the UC, and the DC link.

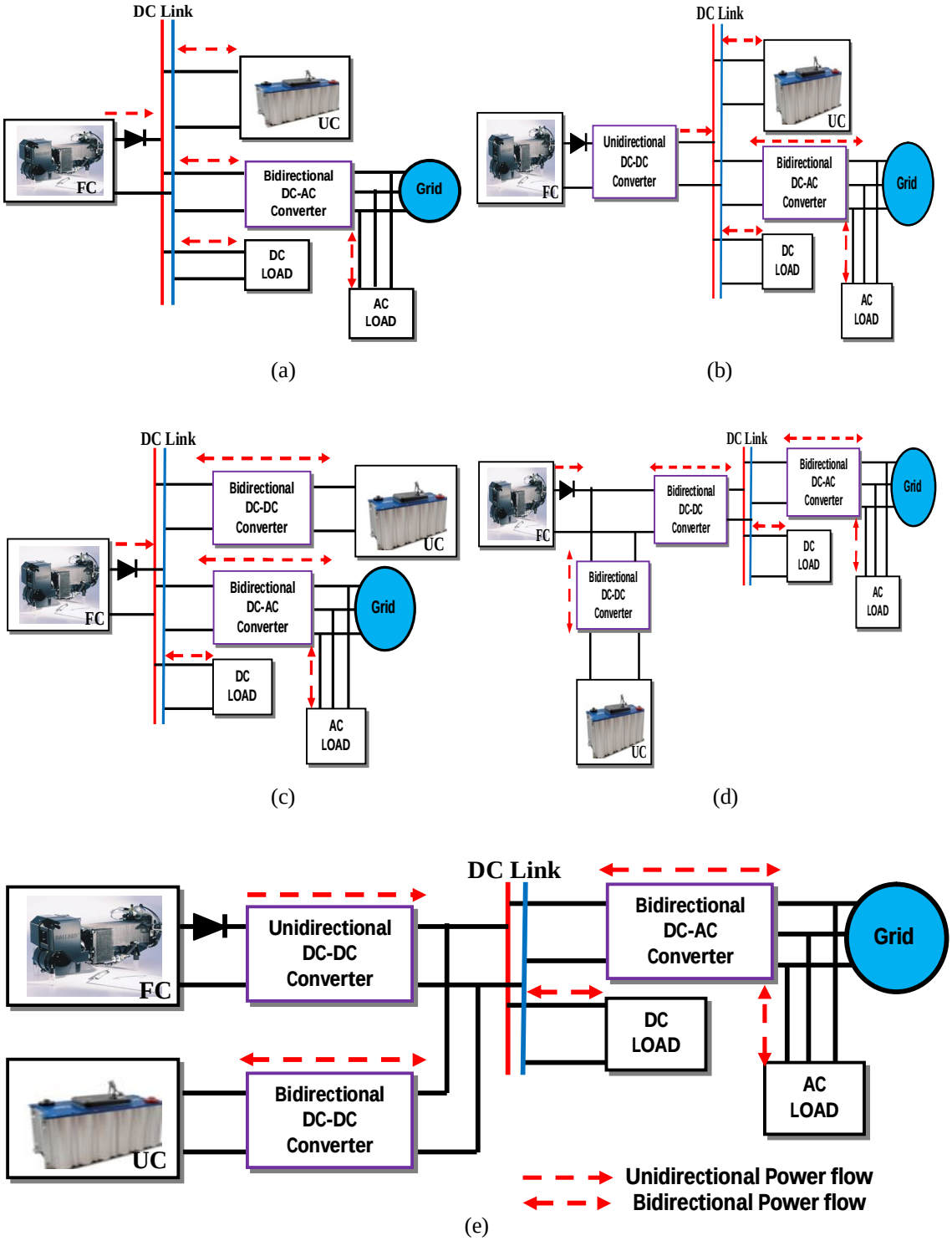


Fig. 2.19 Different UC positions to improve the FC dynamic response and manage the power flow in the FC–UC DC microgrid: (a) passive FC–UC hybrid connection (b) active FC–UC hybrid connection with FC unidirectional converter (c) active FC–UC hybrid connection with UC bidirectional converter (d) parallel–connection of FC and UC through individual DC–DC converters with UC bidirectional converter connected directly to the FC(e) parallel–connection of FC and UC through individual DC–DC converters with UC bidirectional converter connected to the DC link

The UC can be connected to the DC link through a bidirectional DC-DC converter to maintain the charging and discharging of the UC and to regulate the DC link voltage, as depicted in Fig. 2.19c [45-47]. In this configuration, the UC energy buffer is not connected directly to the DC link and therefore a low-voltage UC can be employed. This configuration is widely used for hybrid electrical vehicle applications due to its simplicity and good power flow controllability [47, 48]. However, for the present application this configuration requires a high-voltage FC to fulfill the DC link voltage level (the DC link voltage is up to 650V), which is not a good solution because of the FC cost and reliability[9]. Furthermore, the FC is vulnerable to any rapid dynamic operation of the load since no converter is included to limit the FC current. Therefore, this configuration is not preferable for application in high-voltage power distribution systems.

Another solution to improve the dynamic response of the FC can be obtained by parallel connection of the FC and UC through two different DC-DC converters as depicted in Fig. 2.19d and e. In these configurations the UC converter is connected either to the low-voltage side, as shown in Fig. 2.19d, or to the high-voltage DC link side, as demonstrated in Fig. 2.19e. However, the latter structure provides more control flexibility compared to the first structure. This is because the UC converter in Fig. 2.19d is required to operate with wide input and output voltage variations and it cannot regulate the output voltage since the converter is connected directly across the FC. Nevertheless, both structures can be considered as the best choices for optimal power utilization. With both configurations it is possible to select a low-voltage FC and UC source without having to increase the FC or UC stack size. In addition, they are give a

[9] FCs with high output voltage require a large number of cells in series. If a single cell fails open circuit, the entire stack stops functioning because the current flow is interrupted. This results in a lower FC reliability.

great degree of freedom in power flow controllability [46]. Furthermore, with the configuration in Fig. 2.19e the FC and UC are decoupled from the DC bus so that the input currents can be limited to the acceptable level during rapid transient operation while sustaining the DC link voltage at the required level even for wide input voltage variations. However, with two–converter configurations high losses associated with each converter are expected. Therefore, based on the configuration in Fig. 2.19e, an investigation for efficient DC-DC converter topologies with respect to electrical characteristics of the FC and UC are presented in this Chapter.

2.4.2 Power Flow Management and Control Strategy

Based on the energy conversion architectures described in the last section, the purpose of the hybridisation between the FC and UC in a DC microgrid is to achieve the following:

1. improve the FC output power response,
2. supply power to the fluctuating load whilst taking into account the low FC dynamics, and
3. recover the power generated by the load and store it in the energy storage.

In this way, the whole system would be more efficient and reliable and gives the mechanical devices of the FC sufficient time to adjust, leading to FC operation under more reliable conditions.

The studied configuration of the FC–UC DC microgrid, shown in Fig. 2.19e, has various operational modes according to the conditions of the FC and the UC during autonomous or grid-connected mode. This configuration can be represented as an equivalent circuit as depicted in Fig. 2.20. In this figure the fuel cell–unidirectional DC–DC converter system (FC–UDC) and the ultracapacitor–bidirectional DC–DC converter

system (UC–BDC) in Fig. 2.19e are represented as two DC constant power supplies, delivering the required power to the DC load during autonomous operation.

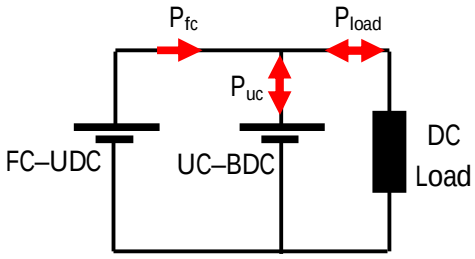


Fig. 2.20 An equivalent circuit of the FC–UC DC microgrid during autonomous operation mode

In this operation the following modes are possible:

- During power demand transient, the UC energy storage delivers the transient power ΔP_{load}. Hence, $P_{uc} = \Delta P_{load}$.
- In constant low–power demand operation, the FC will deliver power to the load and charge the UC storage to recover charge lost during the transient power demand operation. Hence, $P_{fc} = P_{load} + P_{uc}$.
- In constant power demand operation when the UC is fully charged, FC will deliver the power to the load. Hence, $P_{fc} = P_{load}$.
- In the constant high–power demand operation (i.e. load demand > the power delivered by the FC), the FC and UC will deliver the power to the load simultaneously. Hence, $P_{fc} = P_{load} - P_{uc}$.
- In transient energy recovery operation, such as the sudden transition from the load to no-load, the surplus power will be absorbed by the UC storage. Hence, $P_{uc} = -\Delta P_{load}$.

For grid–connected operation, the same modes as above are valid but two more possible modes exist:

- In transient energy recovery operation, if the UC is fully charged the surplus power will be absorbed by the utility gird.
- At constant high–power demand, if the load demand is higher than the maximum power that can be supplied by the FC and UC converter systems, the utility grid will supplement the load power.

To manage the power flow efficiently taking into account the above modes of operation, a control strategy is needed. A number of control strategies have been proposed for the power management of FC–UC hybrid systems [13, 43-47, 49, 50]. The control strategy should manage not only the power flow between the microgrid parts but it should also control the SOC for the UC and maintain the DC link voltage. Hence, the main role of the control strategy of the DC microgrid system can be summarised as depicted in Fig. 2.21.

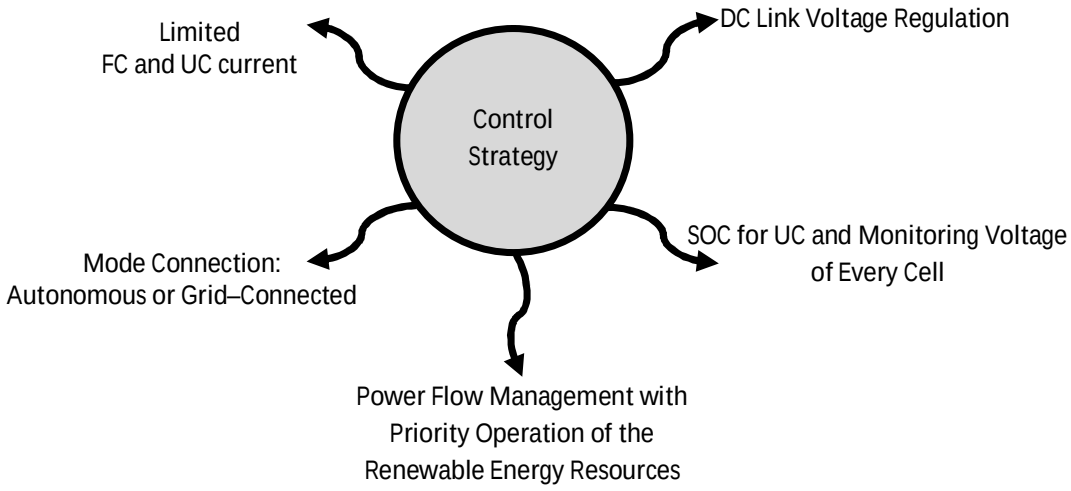


Fig. 2.21 The main role of the control strategy for the FC–UC DC microgrid

In this section, a control strategy for the FC–UC DC microgrid is developed for the power management of the FC and UC sources supplying the load during autonomous operation. Fig. 2.22 shows the basic schematic diagram of the proposed power

management system. In this management system the FC only supplies the base power, while the UC will supply the transient power to the load and regulate the voltage of the DC microgrid. In addition the power management is employed to control the SOC of the UC. The structure of the developed system is composed of the unidirectional converter, bidirectional converter, FC, UC, and closed loop control circuit. The closed loop control circuit comprises a fuzzy logic controller (FLC), a load current detection loop, two inner current loops and an outer voltage loop. The purpose of each control loop is described below:

- Load current detection loop: as indicated in Fig. 2.22, a low-pass filter (LPF) is used to prevent load transients from directly affecting the operation of the FC. Thus, FC responds smoothly to the load demand.
- FC inner current loop which is used to control the input current to the unidirectional converter in order for the FC to deliver the steady–state or average power required by the load and the UC.
- FLC which is utilised to maintain the SOC of the UC within the allowed operating voltage range and to drive the FC current loop with the required charge current reference.
- Voltage control loop to regulate the DC link voltage
- UC inner current loop to limit and control the UC current.

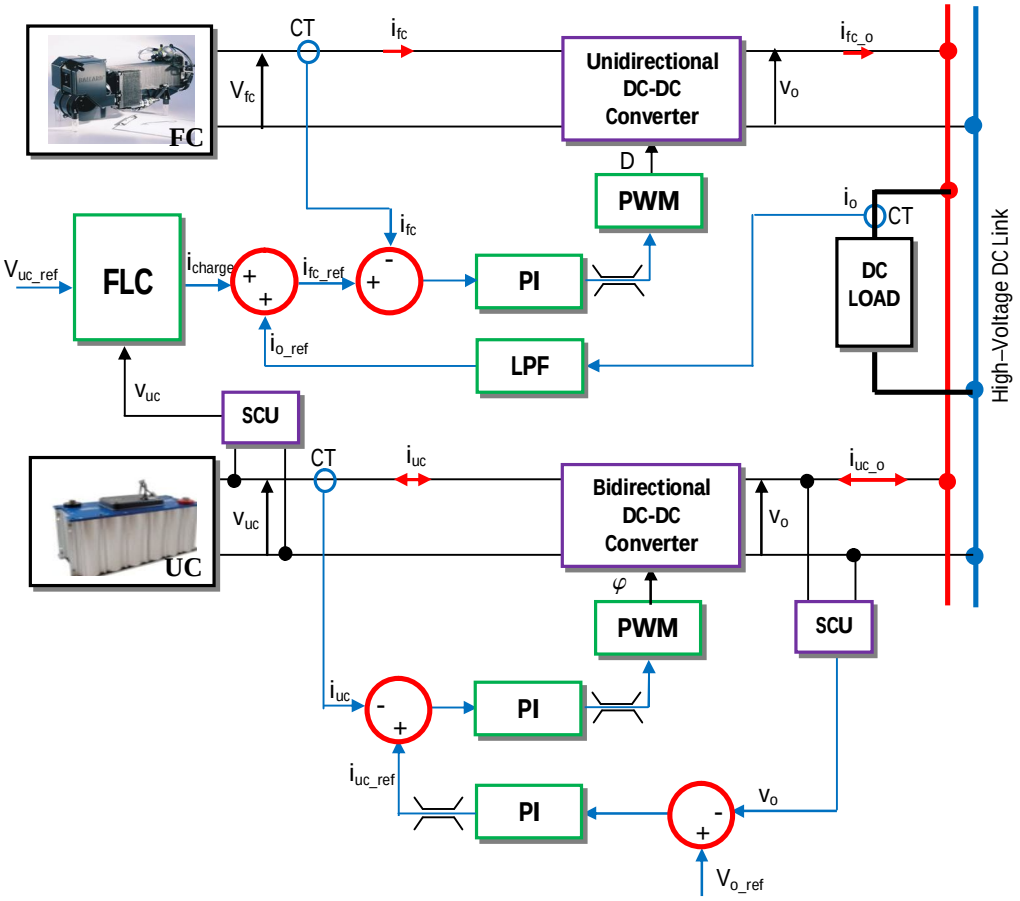


Fig. 2.22 Control scheme for the FC–UC DC microgrid

From the system structure shown in Fig. 2.22, it can be seen that the FC current loop is driven by two current references i_{charge} and i_{o_ref} to control the FC converter. The sum of these generate the reference current i_{fc_ref} which is compared with the actual FC current and the error signal is processed by the FC current controller to control the converter via the duty ratio. In order to eliminate interaction between the FC control loop, the UC control loop and the load current detection loop, a decoupling between the loops must be achieved. For example, to guarantee a smooth response for the FC whilst compensating any power deficiency due to load transients the outer voltage loop must be designed with a higher bandwidth than the cut-frequency of the LPF and the FC current loop. In order for the FC to track the load current demand, once transient

changes have been eliminated, the FC current loop should have a higher bandwidth than the cut-frequency of the LPF.

As mentioned above it is necessary to monitor the UC voltage to control the SOC. When the UC voltage approaches the maximum or the minimum limiting voltage, the FLC will adjust the required current reference i_{charge} and then compared it with the FC current to control the FC converter.

The power management system for a DC microgrid is described here only briefly to clarify how the power flow is managed in the FC–UC DC microgrid. However, further analysis and implementation of the developed control strategy is required.

2.5 Topologies of Fuel Cell and Ultracapacitor Power Converters

In the parallel-connection topology of the FC-UC DC microgrid in Fig. 2.19e, the FC and UC sources are supplying power to the DC bus through two different DC–DC power converters, which are unidirectional and bidirectional respectively. These two converters are the key elements that interface the FC and UC to the rest of the DC microgrid system. A unidirectional converter is preferable for the FC to prevent reverse power, while a bidirectional converter is necessary for the UC to sustain the charging and discharging states of the UC. The main objective of these converters in the FC-UC microgrid is to balance the power flow among the FC, the UC, and the DC link.

As indicated in Sections 2.2 and 2.3, FCs and UCs are typically generating low–voltage DC power. Therefore, step-up DC–DC converters are needed to satisfy the voltage level of the DC link of a DC microgrid. Furthermore, galvanic isolation from the output of FC and UC converters is very desirable where other generators of the DC microgrid system share the same DC bus. Moreover, a converter configuration that combines high

reliability, high efficiency, a high conversion ratio, as well as a low ripple current and low cost is sought.

In addition to the above requirements, the design and selection of the converter should take into account the dynamic response of the FC and UC. Therefore, this section presents an overview of several DC-DC converter configurations that can meet the above requirements for the FC and UC.

2.5.1 Unidirectional DC-DC Converters

Due to the high cost of hydrogen fuel, a high efficiency for the DC-DC converter is very important in hydrogen FC applications. Therefore, a number of different non-isolated and isolated front-end converter topologies for FC applications have been proposed in the literature [51-62]. However, non-isolated converter topologies may not be optimal for FC applications due to direct connection to the high–voltage output side. Also the FC converter must achieve a high boost ratio which may be difficult to accomplish in a non-isolated converter. Even if such converters are able to achieve high step-up voltage ratio, the switching devices will suffer from very high current and voltage stresses [63]. Therefore, a DC-DC converter with a high frequency (HF) transformer is commonly used to provide not only galvanic isolation from the DC bus bar, but also permit interconnection of the DC-DC converters.

Hence, the most interesting topologies for FC applications are the voltage-fed converter (VFC) and the current-fed converter (CFC) with high frequency isolation transformer. Fig. 2.23 a and b show the basic schematic circuit diagrams of the conventional full-bridge VFC and CFC.

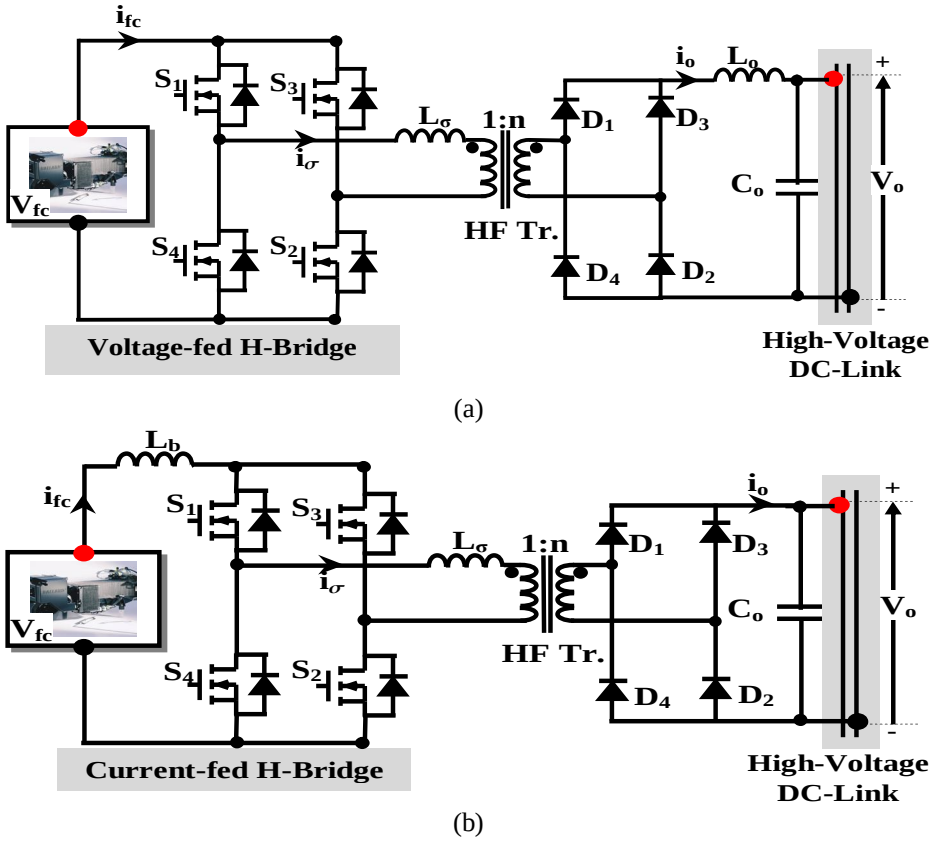


Fig. 2.23 Unidirectional DC–DC Converters [64] (a) voltage-fed topology (b) current-fed topology

The CFC topology has the following advantages over the VFC [64-66]:

- Because of the input inductor, the CFC has an inherently lower input current ripple (at twice the switching frequency) and a unidirectional current flow, thus obviating the need for a series diode (with associated losses) and a bulky input capacitor (usually of the electrolytic type with associated reliability issues).
- The CFC topology has twice the step-up voltage ratio of the VFC, thus reducing the required transformer winding ratio.
- In contrast to the VFC there is no risk of transformer saturation from flux imbalance in the CFC.
- If the switching devices at the same leg of the VFC conduct simultaneously, the current through the switches rises rapidly resulting in device failure and a short

circuit across the input capacitor, which may also damage the FC. Unlike the VFC, a dead time between the switches at the same leg is unnecessary.

- With the CFC an inductor is not necessary in the output filter (see the high-voltage side of Fig. 2.23a and Fig. 2.23b) thus the voltage across the rectifier diodes and the transformer is always equal to the DC link voltage[10].

Therefore, the CFC provides the best solution for achieving most of the properties required for FC applications.

However, three inherent drawbacks are associated with the CFC:

- Unlike the VFC, CFC is a non-minimum phase system; this means that the CFC exhibits a right–half–plane–zero (RHPZ). A RHPZ causes a phase lag at low frequencies which limits the available bandwidth for the CFC resulting in a slower dynamic response for the CFC.
- In practices a CFC presents a high-frequency oscillation produced by the interaction between the transformer leakage inductance and parasitic capacitance of the switching devices. This interaction can lead to excessively high voltage stresses for the switching devices require a higher voltage rating for the switches which may degrade the converter efficiency. Additional circuitry is required to limit or eliminate this effect.
- CFC requires a start-up circuit: due to the input inductance, the initial output voltage at start-up is lower than the reflected input voltage. This results in a high inrush input current before the converter operates in the normal mode. Also, supplementary circuitry must be added to limit the inrush current.

[10] Resonant interaction between the output filter inductance and the parasitic capacitances of the rectifier diodes and the transformer may cause a high-voltage overshoot across the rectifier diodes. Thus, rectifier diodes with a higher voltage rating are required for the VFC, leading to reduce converter efficiency.

To improve the dynamic response of the CFC and therefore reduce the effect of the RHPZ, a smaller input inductance can be employed (with a discontinuous input current and high input ripple as a consequence [67, 68]). Even though, it is has been established in Chapter 4 that the lowest frequency of the RHPZ is much higher than the dynamic frequency of the FC generator. Thus, the slower dynamic response of the CFC due to the RHPZ doesn't have an impact on the FC converter system. A sufficient range is available to design the desired bandwidth for the FC control system (for further details see Section 4.3.2). Nevertheless, elimination or reduction of the effect of the RHPZ is necessary to improve the converter stability.

Based on the above analysis, it can be concluded that, even with the non-minimum phase characteristic, the CFC is suited for the slow–response input sources such as the FC but it is not preferable for fast–dynamic response input sources such as the UC. Therefore, based on the above discussion the CFC has been selected for the FC converter system, while the VFC has been chosen for the UC converter system as will be described later.

To select a CFC suitable for the FC system, several unidirectional CFC configurations are discussed below.

Push–Pull CFC

One of the low-cost DC-DC converter configurations which can be used as a power conditioning unit for the FC generator is the push–pull topology. Fig. 2.24 show the basic schematic circuit of the push–pull CFC [69], where it can be seen the current-fed push–pull converter consists of a boost inductor, two switching devices, a centre-tapped high frequency transformer, and a full-bridge rectifier diodes circuit.

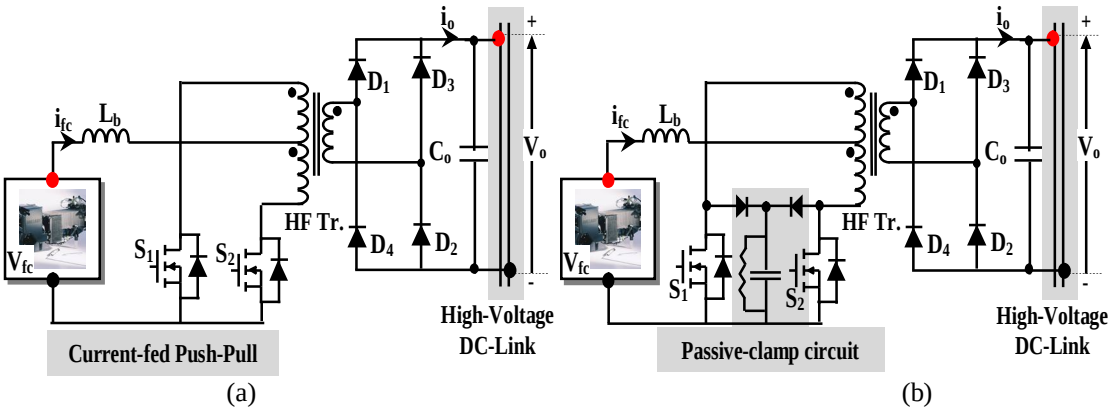


Fig. 2.24 Push-pull CFC for FC system (a) with hard swathing operation [69] and (b) with clamp snubber circuit [70]

The push–pull topology's advantages are a minimal number of switching devices, lower switching losses, simple design, galvanic isolation, and low input ripple current [64]. However, these advantages are achieved at the expense of a reduction in the transformer utilisation (since it uses centre–tapped primary winding), higher conduction losses, and a higher switch voltage stress. Therefore, to protect the switching devices a clamp snubber circuit such as proposed in [70] (see Fig. 2.24b) is needed.

L–Type and Full–Bridge CFC

There are another two possible CFC topologies that can meet the FC requirements: the L-type current-fed converter (LTCFC) also referred to as the half–bridge current–fed converter [71] and the full-bridge current-fed converter (FBCFC) [64]. These two topologies are shown in their basic form in Fig. 2.25 and Fig. 2.23b.

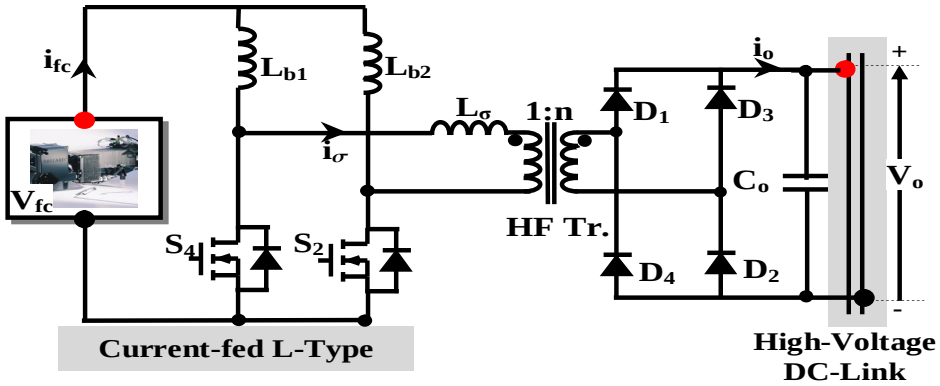


Fig. 2.25 schematic circuit diagrams of LTCFC [71]

Both topologies have an energy storage inductor at the input, an HF isolation transformer and a diode rectifier bridge with smoothing capacitors at the output. Both configurations provide an inherent boost action, which results in a lower transformer ratio and a subsequent reduction in the leakage inductance, which improves the converter's efficiency. Compared to the FBCFC topology (Fig. 2.25b), the LTCFC (Fig. 2.25) has a smaller number of active devices but requires two DC inductors which carry a current ripple at the switching frequency, while the single inductor of the FBCFC has a current ripple at twice the switching frequency. Both configurations act a controlled current source and are therefore suitable for a FC generator.

Major drawback of these configurations are hard switching operation and voltage spikes at turn–off due to the transformer leakage inductance which result in high conduction and switching losses. Consequently, the operating efficiency and the reliability of the converter will be reduced. Additional circuitry must be added to reduce or avoid the above effects.

CFC with Voltage–Doubler Circuit

The size of the HF transformer, the efficiency of the converter, and the voltage stress across the active devices can be improved by reducing the turns ratio of the transformer. For that reason, a voltage–doubler FBCFC with a centre-tapped HF transformer is

proposed in [72] consisting of two rectifier diodes and two output capacitors as shown in Fig. 2.26.

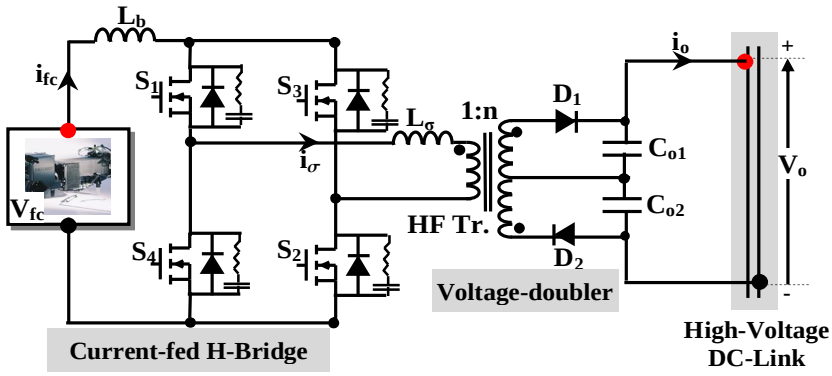


Fig. 2.26 FBCFC with voltage-doubler rectifier diode [72]

The important advantages of this configuration are described below:

1) In addition to the normal boost operation of the CFC, the voltage–doubler rectifier diode doubles the voltage conversion ratio of the CFC; this is an important feature for CFC's fed from low input voltage sources, such as a fuel cell.

2) Employing components with a lower voltage rating (and hence a lower on-state resistance or voltage drop) reduces the conduction losses at both sides of the transformer and simplifies the converter structure.

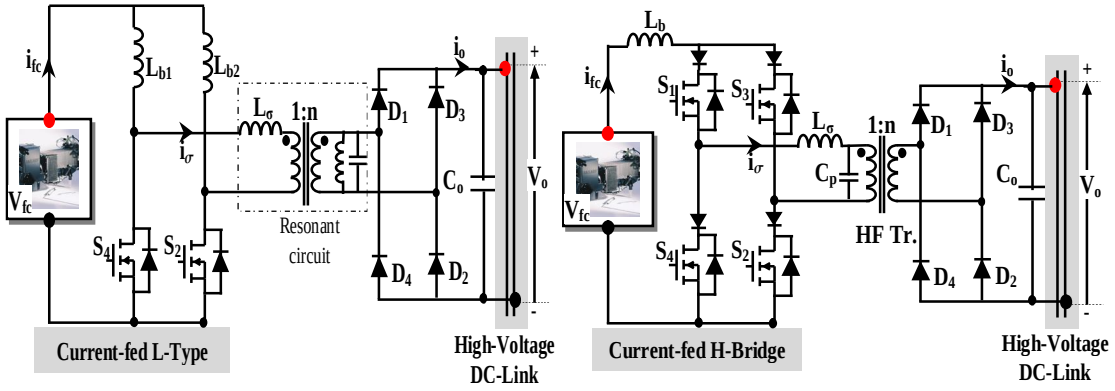
3) Because only half of the output voltage is applied across the secondary winding of the isolation transformer, a lower turns ratio can be afforded which not only reduces the total leakage inductance but also simplifies interleaving of the primary and secondary windings.

The main drawback of this configuration is that the switch devices still suffer from severe voltage stress at turn-off for two reasons: the switches operate with hard switching and the secondary side of the transformer uses two windings, leading to a higher leakage inductance and lower transformer utilisation which result in a reduction

of converter efficiency.

Current-Fed Resonant Converter

In [73, 74] resonant version of the L-type and full-bridge current-fed converters with zero–current switching (ZCS) are proposed, as shown in Fig. 2.27a and Fig. 2.27b, to reduce the switching losses and the switches voltage stress of the CFC and thus improve the converter efficiency.



(a) (b)

Fig. 2.27 Current–fed resonant converter (a) LTCFC [74] and (b) FBCFC configuration [73]

The resonant LTCFC ZCS converter utilises the leakage inductance, magnetising inductance and parasitic capacitance of the transformer to achieve ZCS and reduce the voltage spikes across the switches. An additional advantage of this configuration is that the rectifier diodes are operated with ZCS. The same improvements can also be achieved with the resonant full-bridge current-fed converter. The converter shown in Fig. 2.27b is an example for this configuration. In the latter configuration diodes are connected in series with the switching devices to prevent current flowing through the anti-parallel diodes of the switches, thus reducing circulating currents. However, the series-connected diodes will increase the number of components and cause higher conduction losses.

Generally, the resonant converters increase the complexity of the converter design and required additional components. In addition the operation of these configurations is a function of the load. Furthermore, in general they are generating a significant amount of circulating current in the full bridge which adds to the conduction losses of the converter.

Phase-Shifted CFC

A phase-shifted full-bridge CFC has been proposed in [75] to achieve ZCS for the bridge switches, as depicted in Fig. 2.28.

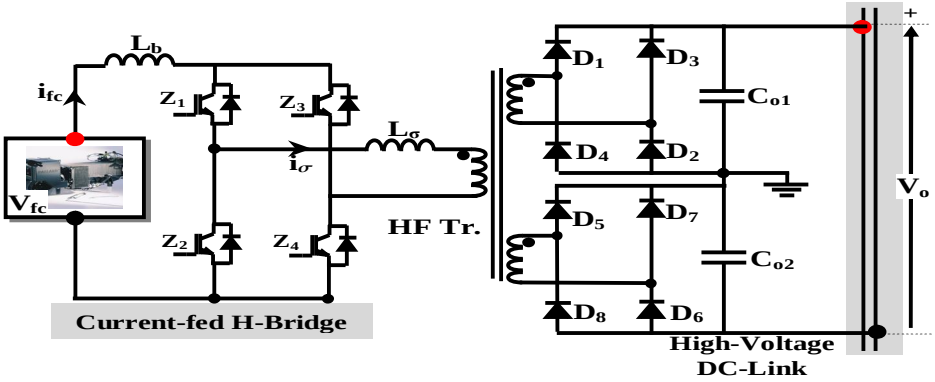


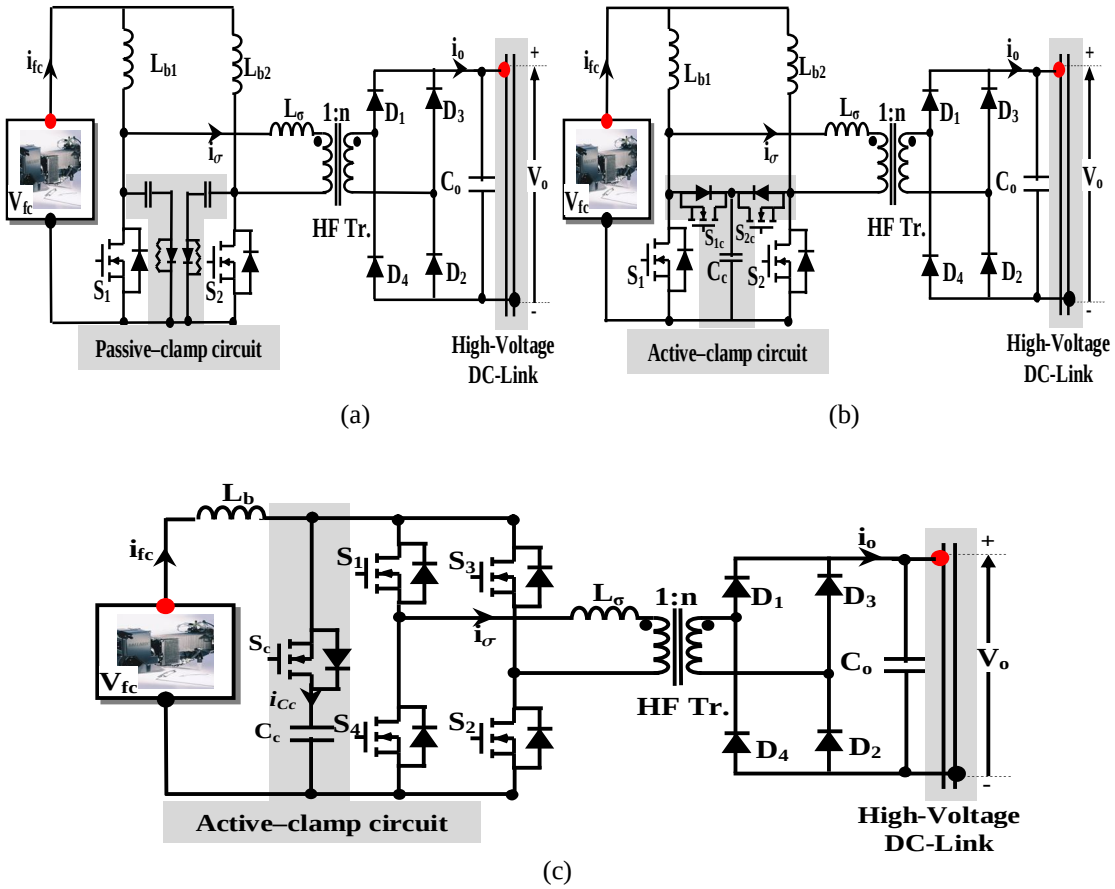
Fig. 2.28 Phase-shifted FBCFC with reverse blocking IGBTs and two full-bridge rectifier diodes [75]

In this configuration, the switch devices must provide a reverse-voltage-blocking capability. Therefore, this configuration is using reverse blocking IGBTs to avoid using series diodes that are employed with the configuration in Fig. 2.27b to achieve ZCS. However, reverse blocking IGBTs are more expensive than conventional IGBTs and are not available for low input voltage applications.

CFC with Voltage Clamp Circuit

Passive or active clamps have been presented in [56, 58-60, 76-78] to achieve zero–voltage switching (ZVS) and reduce or avoid the high voltage stress for the converter switches. Fig. 2.29a and b show the LTCFC configurations with passive and active

clamp circuits , while Fig. 2.29c shows the lay-out of the FBCFC with an active–clamp circuit placed directly across the input bridge.



(a) (b)

(c)

Fig. 2.29 Schematic circuit diagrams of (a) LTCFC with passive–clamp circuit [78] (b) LTCFC with active–clamp circuit [57] and (b) FBCFC with active–clamp circuit [76]

However, in Fig. 2.29a the energy stored in the capacitance of a passive clamp is dissipated on the snubber resistor; such a clamp will therefore reduce the converter efficiency.

Active clamp circuits across the converter switches can be used to absorb the resonant leakage energy and recover it to the load whilst clamping the voltage across the switching devices. This has the additional advantage of operating the main switches with ZVS at turn-on, thus improving converter efficiency. Compared to the active clamp FBCFC (Fig. 2.29c), the main drawbacks of active clamp LTCFC configuration

(Fig. 2.29b) are the use of more passive components and the need for two active clamp circuits, thus increasing the complexity of the PWM control circuit.

CFC with Start-Up Circuit

As indicated in the previous section the CFC with active clamp circuit can achieve high efficiency because the reduction in voltage stress and of the switches soft–switching operation. Despite this, this CFC has a start–up problem. At start–up the output filter capacitor (C_o) of the CFC is being charged from zero voltage while the FC voltage is at its nominal value. Thus, the FC current is uncontrollable during start–up. To avoid over-current in the start-up stage, an additional circuit (Fig. 2.30) or an extra control algorithm at the start–up is needed as presented in [79, 80].

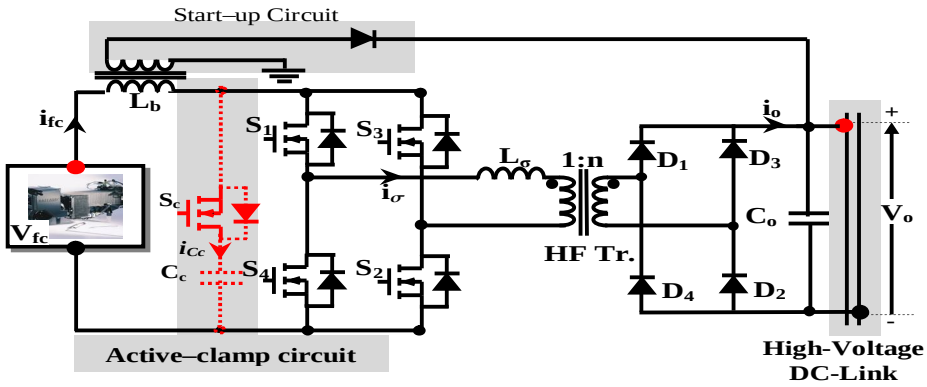


Fig. 2.30 Start-up configuration for FBCFC with optional regenerating clamp stored energy [79], [81]

An additional flyback winding have been proposed in [81], as shown in Fig. 2.30 also to recover the energy stored in the clamp capacitor directly to the load. However, this additional converter suffers from discontinuous input current which is detrimental for the FC system.

Multi–Phase and Interleaved CFC

For high–power applications and further reduction in the FC ripple current, a multi–phase and interleaved CFC, controlled by a phase-shifted PWM, has been proposed in

[82] and [83]. An example of a multi–phase CFC consists of a three–phase three–leg configuration is depicted in Fig. 2.31.

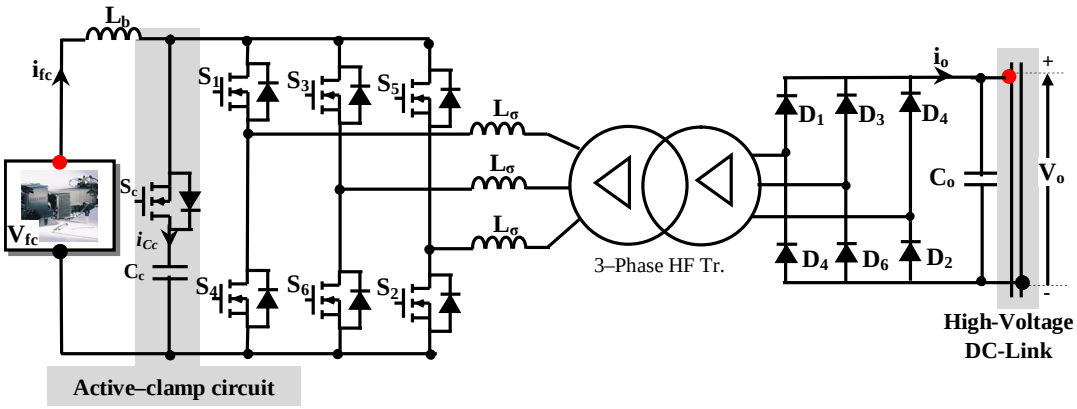


Fig. 2.31 High–power three–phase three–leg active clamp CFC [82]

With the multi–phase CFC the size of the boost inductor is reduced and the output filter inductor is eliminated. Owing to the multiphase topology, the converter decreases the conduction losses by distributing the RMS current through the phase switches and transformer windings. By interleaving two CFCs, as proposed in [83], with parallel input and series output connection, a reduction in the FC current ripple and output voltage ripple can also be achieved. The main drawbacks of these topologies are that they required a high number of active and passive parts.

Comparison of CFC Configurations

Among the different CFC configurations discussed above, four CFC configurations are considered in this work for comparison with the proposed CFC which will be introduced in the next Chapter. These CFC configurations are listed below:

- Conventional FBCFC with full–bridge rectifier diode without active–clamp circuit (see Fig. 2.23b) which is denoted as “Config.1”

- FBCFC with voltage–doubler rectifier diode without active–clamp circuit (see Fig. 2.26) which is denoted as “Config.2”
- Active–clamp FBCFC with full–bridge rectifier diode (see Fig. 2.29c) which is denoted as “Config.3”
- Active–clamp LTCFC with full–bridge rectifier diode (see Fig. 2.29b) which is denoted as “Config.4”

Table 2.3 summarises the main features of these CFC configurations.

TABLE 2.3
A BRIEF COMPARISON BETWEEN DIFFERENT CFC CONFIGURATIONS

Converter Configurations	**Components**	**Inductor current ripple frequency**	**Output voltage V_o**	**Transformer turn ratio n**	**Comments**
Config.1	Four main switches Four diodes One capacitors One inductor	Twice the switching frequency	$\frac{n V_{fc}}{1-D}$	Lower than VFC	➢ Simple PWM control circuit. ➢ Hard switching operation
Config.2	Four main switches Two diodes Two capacitors One inductor	Twice the switching frequency	$\frac{2 n V_{fc}}{1-D}$	Half the ratio of Config.**1**	➢ Lower cost and smaller size because it is used lower n. ➢ High over-voltage spikes.
Config.3	Four main switches One clamp switch Four diodes Two capacitors One inductor	Twice the switching frequency	$\frac{nV_{fc}}{1-D}$	Lower than VFC	➢ ZVS for all switches. ➢ Clamp voltage is function of load
Config.4	Two main switches Two clamp switches Four diodes Two capacitors Two inductor	Same as the switching frequency	$\frac{n V_{fc}}{1-D}$	Lower than VFC	➢ Complex PWM control circuit. ➢ ZVS for all switches. ➢ More passive components.

2.5.2 Isolated Bidirectional DC-DC Converters

A bidirectional DC–DC Converter (BDC) is used in a FC–UC microgrid system to provide an interface between the low-voltage UC storage and the high–voltage DC bus and to manage the power flow between the FC generator, the UC storage and the load. Several voltage–fed and current–fed isolated BDC topologies can be employed to fulfil the requirements for interfacing the UC storage with the FC and the DC link of a DC microgrid. However, as indicated in Section 2.5.1, the voltage–fed isolated BDC topology has been selected as a power conditioning unit for the UC storage in this work, based on the UC characteristics.

The principle operation of a BDC and an overview of suitable voltage–fed BDC topologies are presented next.

2.5.2.1 Principle of Operation

In principle, the isolated BDC can be represented as two DC–AC converters C_A and C_B connected to two DC sources V_A and V_B and interfaced through an inductor L_t as illustrated in Fig. 2.32a. In order to transfer power, the instantaneous output voltages v_A and v_B must be supplied by the converters C_A and C_B to the inductor L_t. Hence, the BDC can be replaced by two independent AC voltage sources v_A and v_B connected through inductor L_t as shown in Fig. 2.32b.

To clarify the BDC operation, the voltage and current relationships of the BDC can be analysed using the phasor diagram of the fundamental components, depicted in Fig. 2.32c.

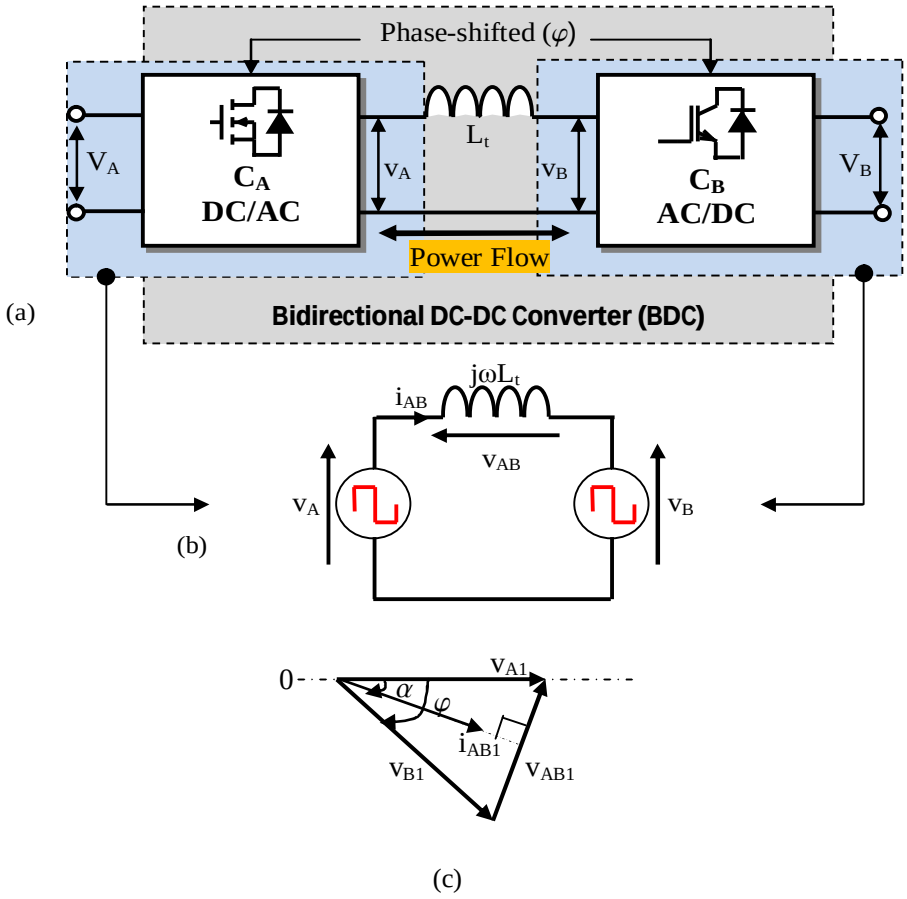


Fig. 2.32 Operating principle operation of a BDC (a) simplified block diagram (b) equivalent circuit model (c) phasor diagram of the fundamental components of the voltages and current

Based on the fundamental components, the fundamental power flow between the two AC sources in Fig. 2.32c can be written as

$$P_{AB} = \frac{\hat{V}_{A1}\hat{V}_{B1}}{2X_{Lt}} \sin\varphi \qquad (2.5)$$

where $\hat{V}_{A1}$ and $\hat{V}_{B1}$ are the amplitudes of the fundamental voltages of v_A and v_B, φ is the phase-shift between v_A and v_B , and $X_{Lt} = \omega L_t$.

For a square waveform: $\hat{V}_{A1} = \frac{4V_A}{\pi}$,$\hat{V}_{B1} = \frac{4V_B}{\pi}$.

Referring to (2.5) the magnitude and direction of the fundamental power in the BDC is determined by the phase-shift φ. Hence, the power transfers from the source v_A to the

source v_B in case v_B is lagging v_A (i.e. φ is larger than 0^0) and the power transfer reverses in case v_B is leading v_A (i.e. φ is smaller than 0^0).

2.5.2.2 BDC Overview

In recent years, several voltage–fed BDCs for the UC storage have been proposed. The most interesting topology for the bidirectional applications is the dual H–bridge BDC presented in [84]. The dual H–bridge BDC uses a phase-shift between the bridges to control the power flow through a high frequency isolation transformer. Typically, a dual H–bridge BDC (Fig. 2.33) is preferred in high-power applications because of its minimal voltage and current stresses, utilisation of the transformer's leakage inductance, low switching losses, and low ripple currents at the output filter [85].

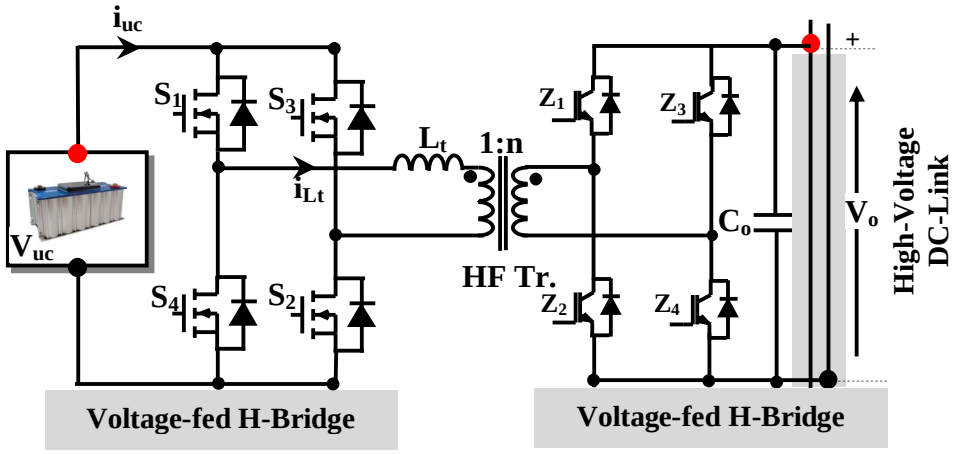


Fig. 2.33 Dual H–Bridge Bidirectional converter [84]

The dual half–bridge BDC topology has also been considered for the UC particularly for electric vehicle application [86, 87]. The advantages of the dual half–bridge BDC, shown in Fig. 2.34, is the lower parts count (reduces hardware effort regarding gate drivers) and lower voltage stress. However, the RMS current ratings of the switching devices are twice the RMS current ratings of the switches employed for the H–bridge. This is a serious drawback in particular for the low–voltage side.

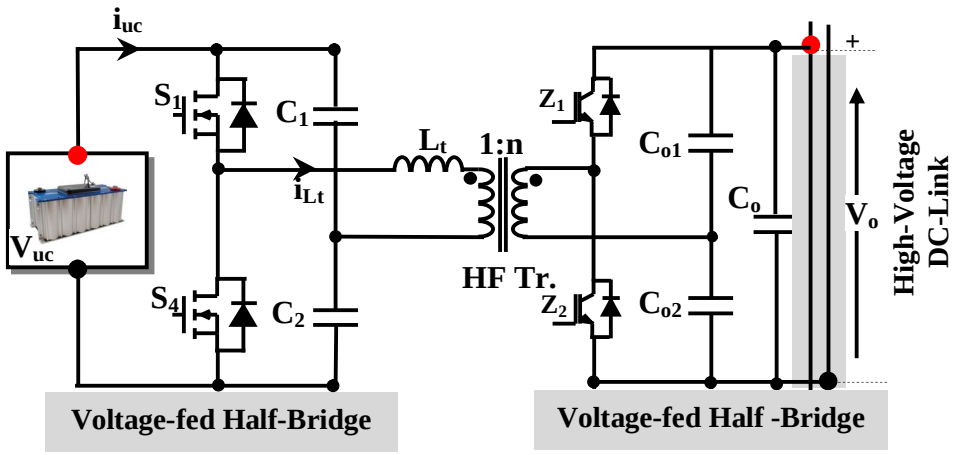


Fig. 2.34 Voltage–fed dual half–bridge bidirectional converter [86]

A BDC with H–bridge at the low–voltage side and push–pull topology at the high–voltage side was proposed in [88]. The main advantages of this topology are the lower voltage stress on the switches and lower number of switching devices. However, to connect the push–pull circuit (as indicated in Fig. 2.35) a tapped secondary winding is required and this leads to ineffective transformer utilisation.

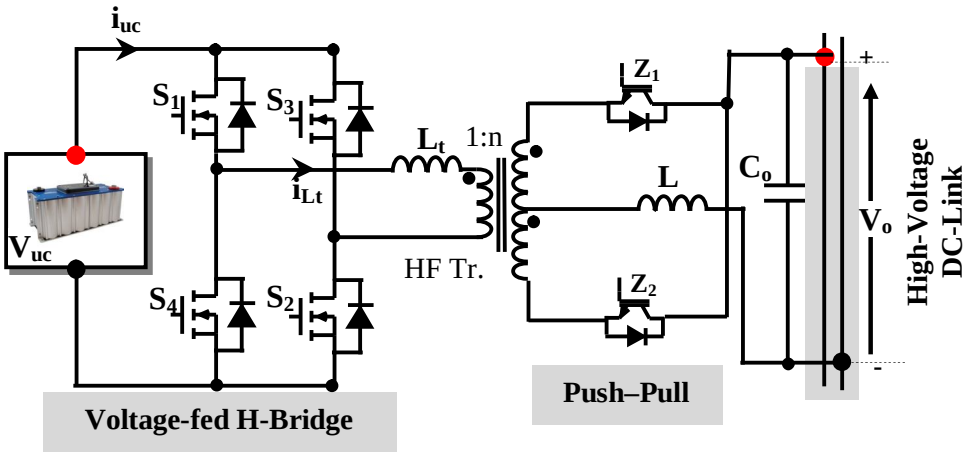


Fig. 2.35 Voltage–fed H–Bridge and push-pull Bidirectional converter [88]

For this configuration, the RMS current ratings of the switches in the H–bridge are the same of the dual H–bridge configuration, while the voltage ratings of the push–pull switches are twice the voltage ratings of the switches utilised for the dual H–bridge

configuration. A similar configuration has been proposed in [89], where the H–bridge connects to the push–pull circuit through two transformers with series–connection to eliminate the output inductor and achieve ZVS. However, this configuration increases the complexity of the converter design. Also in [90] a combination of half–bridge and push–pull topologies are employed. This topology has only 4 switching devices and can provides the desired bidirectional flow of power for UC charging but on the account of a high RMS current via the switches at the low–voltage side and high–voltage stress across the switches at the high–voltage side in comparison to the dual H–bridge configuration.

A perfect soft switching BDC should have the features as ZVS for the primary side switches and ZCS for the output rectifier switches, in both power flow directions, to minimise the switching losses. For that reason, resonant circuits can be added to the BDC as shown in Fig. 2.36 [91].

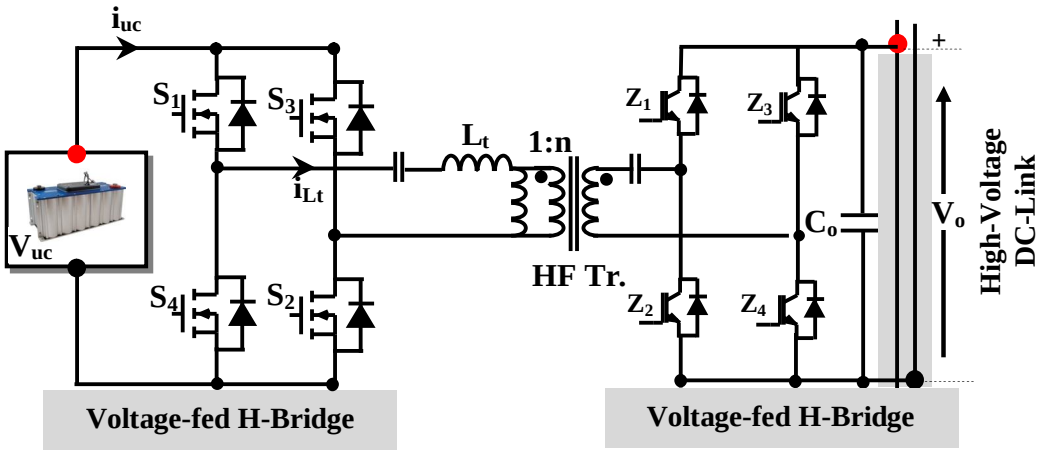


Fig. 2.36 Dual H–Bridge Bidirectional resonant converter [91]

Series, parallel, and series–parallel resonant BDCs can also be employed. However, compared to the dual H–bridge BDC, a considerably higher transformer VA rating is required due to the increase of circulating current in the high–frequency resonant

network (in particular with respect to the required input and output voltage ranges and the required constant switching frequency operation). Taking into account the requirement for additional passive components, the resonant BDC converter is considered to be less attractive than the dual H–bridge BDC and is therefore not investigated here.

One of the promising BDC topologies that has attracted increasing research interest recently is the multiport BDCs [92]. This topology uses multi–winding transformer to interface the UC, FC and the load and control them together in a single power processing stage. Fig. 2.37 depicts the basic block diagram of this topology.

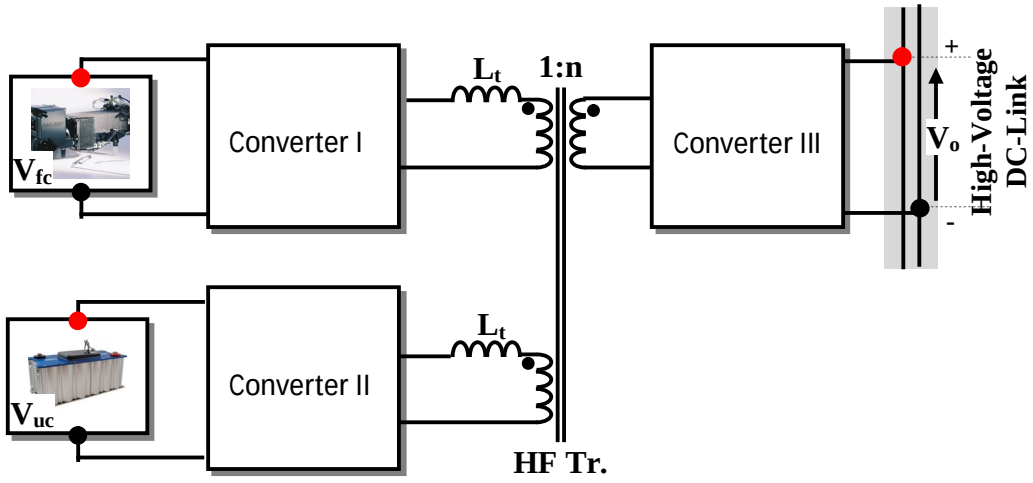


Fig. 2.37 Three-port bidirectional DC–DC converter

Each converter in this topology could potentially use a voltage-fed or current-fed H-bridge, half-bridge or push-pull configuration. The power can be transferred by phase shift between the high-frequency voltages presented to the windings. With multiport BDCs, all the UC, FC sources and loads are galvanically isolated. However, unlike the present application, this topology is most suited for electric vehicle applications where all sources and loads are in close vicinity.

2.6 Conclusions

In addition to the electrochemical reaction inside the cell the fuel cell voltage–current characteristics are determined by mechanical devices, which are used for maintaining the air pressure, the temperature, and the humidity in the cell. Therefore, the FC has a slow dynamic power response with respect to certain transient load requirements. To compensate for the slow transient response of the FC, an auxiliary energy storage device is required. One of the promising energy storage devices is the ultracapacitor. This can be used to interface the UC with the FC to form (part of) a DC microgrid. A comparison has been presented in this Chapter of various FC–UC hybrid connections. Parallel-connection of the FC and UC through individual DC–DC converters has been shown the best topology with respect to management of the power flow. Various voltage–fed and current–fed isolated and non-isolated DC–DC converter topologies can be used to interface the FC and the UC to the DC bus of a DC microgrid. It has been demonstrated that unidirectional isolated current–fed DC–DC converter has attractive features for the FC source, while for the UC the bidirectional isolated voltage–fed DC–DC converter is most promising with respect to the achievable converter efficiency, the achievable power density (due to the low number of inductors and capacitors), and the fast–response performance.

Therefore, a modified FC current–fed converter based on a combination of active clamp circuit and voltage–doubler is reported in Chapter 3. To improve the achievable efficiency of the BDC for a UC and optimise the control power flow, a new optimal modulation scheme presented in Chapter 6.

Chapter Three

Fuel Cell CFC with High Voltage Step-Up and Low Switch Voltage Ratings

3.1 Introduction

The selection of the DC-DC converter topology for FC power conversion systems requires dealing with FC source specifications, such as low voltage and high current whilst maintaining low input current ripple, high voltage conversion ratio, and high efficiency. As mentioned in Chapter 2, the CFC can satisfy all these requirements simultaneously.

However, one of the CFC drawbacks that is the voltage stress across the switching devices from hard-switching operation which also results in reduced converter efficiency. Therefore, as explained in Chapter 2 most of the CFC configurations proposed in the literature are mainly focused on how to reduce the switching losses of the converter's switches. This is achieved either by using an additional resonant circuit [55, 61, 62, 93-98], an RC snubber circuit or an active clamp circuit [54, 57-61, 76-78, 99-101]. These configurations, however, have at least one of the following drawbacks:

i. A considerable amount of circulating current in the bridge switches which add to the converter conduction losses and contribute to the peak current stress of the bridge switches, for example in resonant converters

ii. Higher voltage ratings of the switching devices with associated higher on-resistance increasing the conduction losses as a consequence

iii. Energy circulation through the bridge switches[1] resulting in increased conduction losses in the bridge switches

iv. High dissipated power and lowest efficiency due to use passive snubber circuit.

Therefore, in this Chapter a high efficiency CFC with a high voltage step-up and low voltage rating of the switches is proposed that doesn't suffer from the above disadvantages. As shown in Fig. 3.1, the proposed converter consists of an active-clamp and a voltage-doubler circuit with an untapped secondary winding transformer. By combining the voltage-doubler circuit with an active clamp circuit the proposed converter can achieve soft-switching and low conduction losses as well as low input current ripple, a low circulating energy, and a high efficiency over the whole load range, which is very attractive for a low-voltage FC generator.

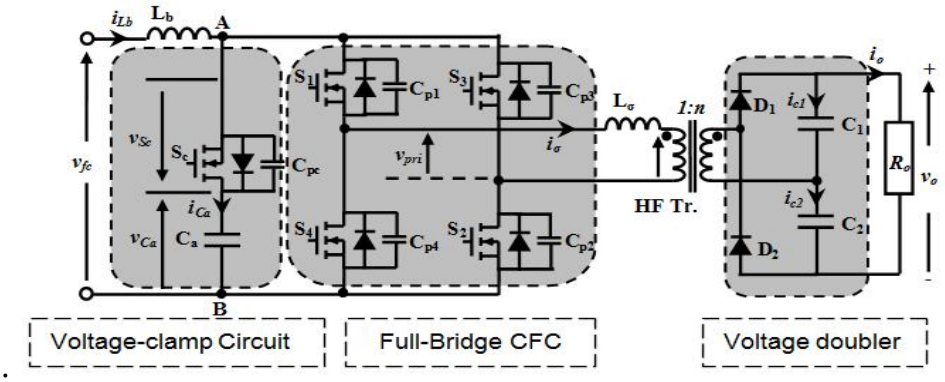


Fig. 3.1 Schematic diagram of the proposed FBCFC

The steady-state analysis of this converter is first explained and analysed, and the procedure to further improve the converter efficiency is demonstrated in detail. Experimental results obtained from an existing prototype converter and the new

[1] Since the circulating energy caused by the clamp capacitance varies with the square of the capacitor voltage V_{Ca}.

prototype converter with an improved layout is presented. Finally, a comparison of the proposed converter in respect to other competing CFC configurations is made and measurement results are presented and compared with the results of detailed simulation.

3.2 Steady-State Analysis of the Proposed CFC

To better help demonstrate the features of the proposed CFC, it is necessary to start from the description of circuit operation and derivation of the equivalent circuits for each operating mode. The converter has been analysed and implemented based on the 3kW converter prototype with the following specifications: V_{fc} = 42-26V, V_o = 650V, n=7.4, f_s = 50 kHz, L_b = 475μH, C_1=C_2=500μF, L_σ =2 μH while the FC output power P_o =1.2kW[2].

3.2.1 Operational Principle

This Section details the operational analysis of the proposed CFC for the entire switching cycle (T_s). The timing signals and waveforms of various voltages and currents for the converter circuit in Fig. 3.1 are shown in Fig. 3.2. The full switching cycle has been divided into two symmetrical half switching cycles ($0.5T_s$), as shown in Fig. 3.2 which only differ in the way that the output capacitors C_1 and C_2 are charged; only the first eight intervals are described here. In order to simplify the analysis, the following assumptions have been made:

1. In order to keep sufficient energy stored in the boost inductor so that the converter is capable to step-up the FC voltage to the required level, there must be a period of overlap (T_E) for the diagonal switches of the full-bridge equal to

[2] The most important symbols and abbreviations are defined in Appendix “Glossary and Terms”.

$$T_E = \frac{T_{on} - T_{off}}{2} \tag{3.1}$$

where T_{on} and T_{off} are the turn-on and turn-off periods of the bridge switches.

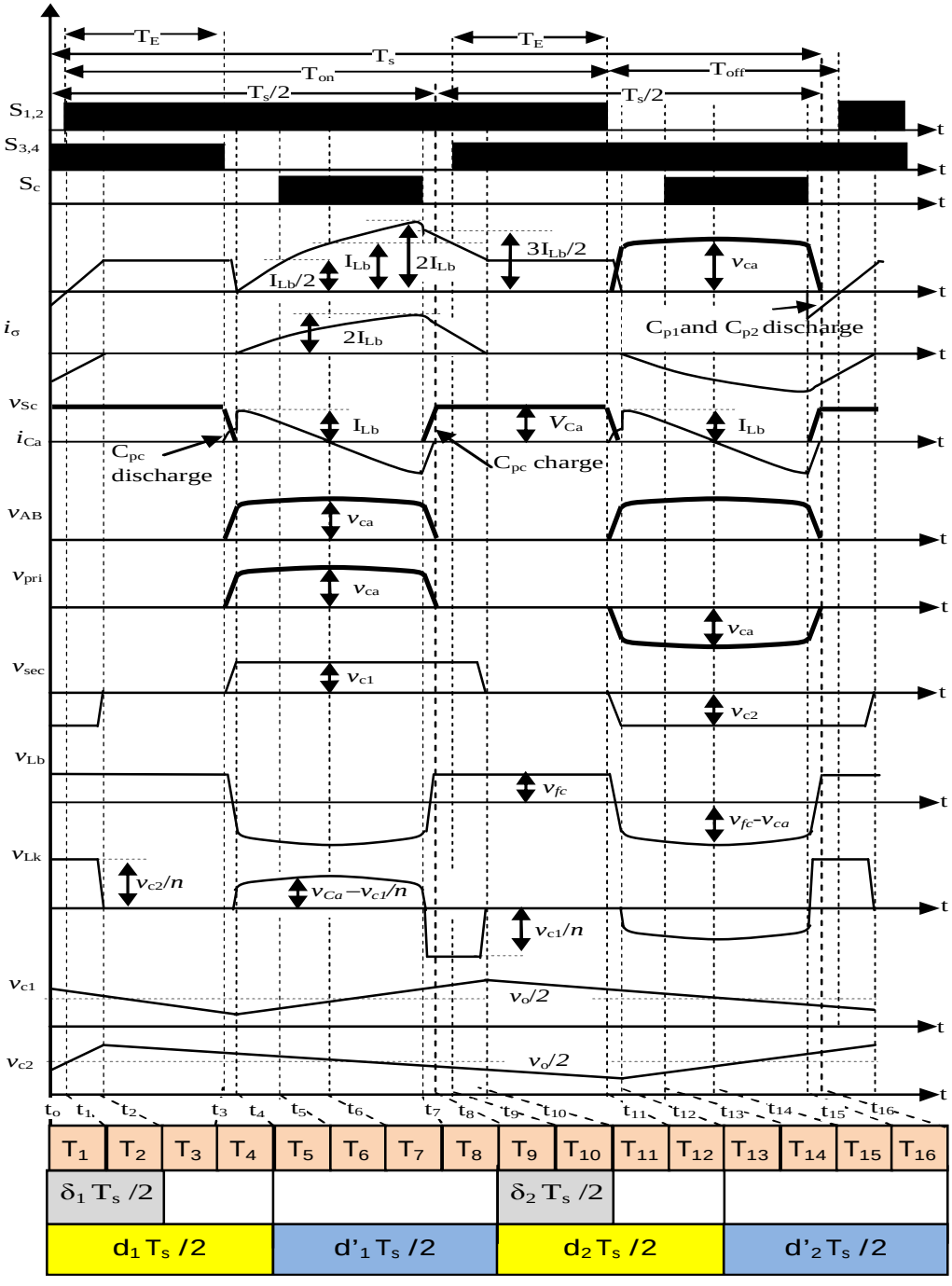


Fig. 3.2 Gate signals, voltage, and current waveforms of the proposed FBCFC

This means that the turn-on period T_{on} is always greater than 50% of the switching time period T_s and the diagonal switches (S_1~S_2 or S_3~S_4 in Fig. 3.1)

should not all turn off at the same time.

2. The transformer magnetising inductance is ignored.
3. The leakage inductance of the secondary side is combined with the leakage inductance of the primary side into the transformer leakage inductance (L_σ).
4. The on-resistances (R_{on}) of the MOSFETs (S_1~S_4) and rectifier diodes voltage drops are neglected.
5. Initially all parasitic inductances in the switching devices and circuit wiring have been neglected.
6. The output voltage ripple across C_1 and C_2 is small over a switching cycle (i.e. the output voltage V_o is assumed to be constant).
7. The clamp capacitance C_a is much greater than the parasitic capacitance (C_{p1}~C_{p4}) of the bridge switches.
8. The boost inductor is considered large enough to be making the input current (i_{Lb}) continuous (CCM[3]).

However, the MOSFETs parasitic capacitances and anti-parallel diodes are not excluded.

The equivalent circuit for each mode in the first half-cycle (i.e. T_1-T_8) is given in Fig. 3.3.

[3] CCM requires that the inductor current does not reach zero.

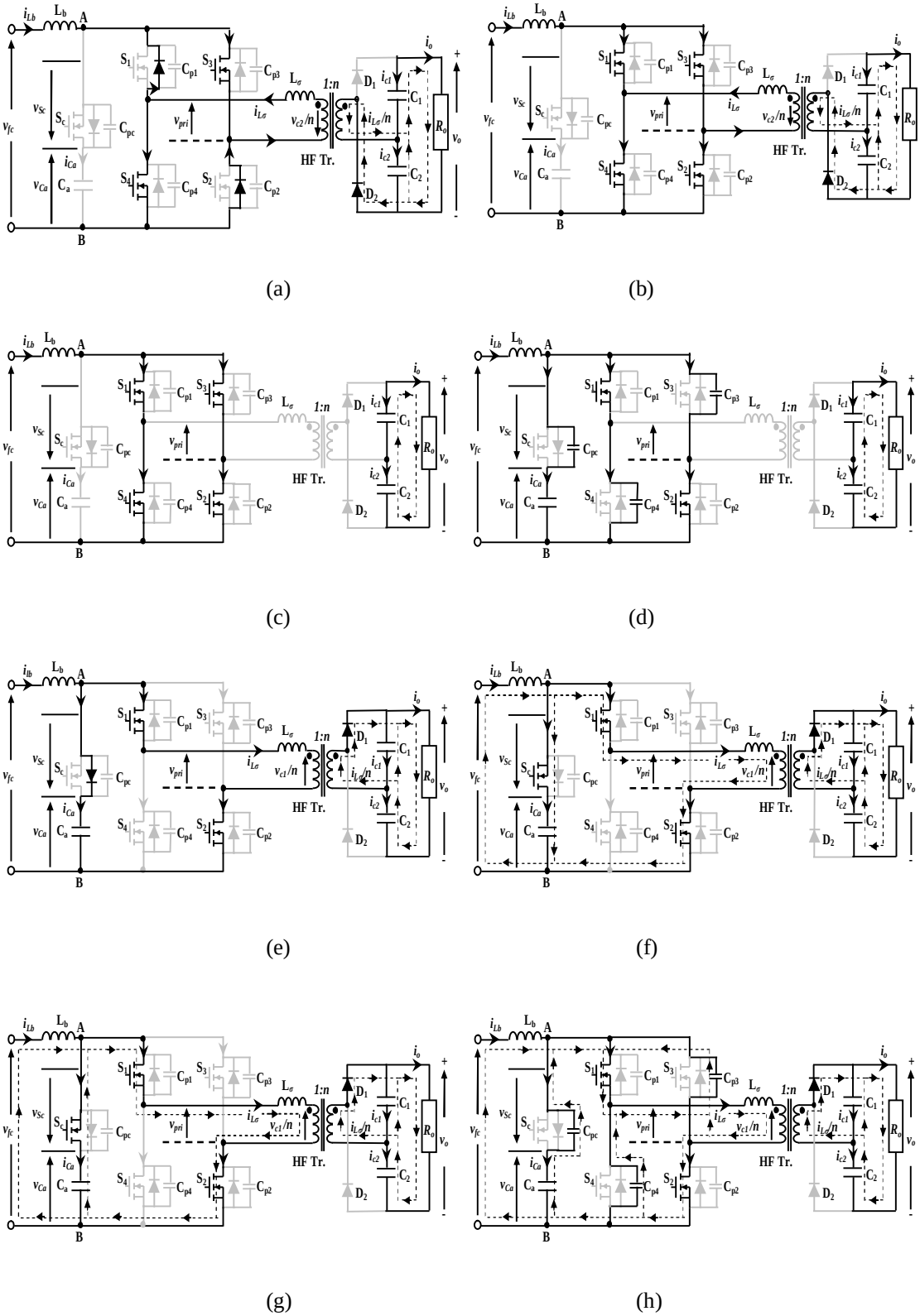


Fig. 3.3 Detailed equivalent circuits of the proposed current-fed converter for each operating state. (a) (T_1: ∈ (t_0 , t_1)), (b) (T_2: ∈ (t_1 , t_2)), (c) (T_3: ∈ (t_2 , t_3)), (d) (T_4: ∈ (t_3 , t_4)), (e) (T_5: ∈ (t_4 , t_5)), (f) (T_6: ∈ (t_5 , t_6)), (g) (T_7: ∈ (t_6 , t_7)), (h) (T_8: ∈ (t_7 , t_8))

The switching operational modes of the converter can be distinguished as following:

Mode T_1: As shown in Fig. 3.3a, at t_0 the parasitic capacitances C_{p1} and C_{p2} will be discharged, and the anti-parallel diodes of S_1 and S_2 start conducting. Therefore, S_1 and S_2 can be turned on with zero voltage at the next mode. At the beginning of this mode, the voltage across the clamp branch (v_{AB}) has already declined to zero and the blocked voltage (V_{Sc}) go up to:

$$V_{Sc} = v_{Ca} = V_{Ca} \approx \frac{V_o}{2n} \tag{3.2}$$

where v_{Ca} and V_{Ca} are the instantaneous and average voltage across the clamp capacitor respectively.

Mode T_2: In this interval, S_1~S_4 will all be conducting but leakage inductance still delivers energy to the secondary side and the current in each leg of the bridge is equal to half of the average FC current. Fig. 3.3b shows the equivalent circuit of this mode. Although all the bridge switches are conducting, the secondary voltage is not equal to zero due to the primary current ($i_{L\sigma}$) is still circulating. This current is equal to

$$i_{L\sigma}(t) = -\overline{I_{Lb}} + \frac{V_{C2}}{nL_\sigma}(t - t_1) \tag{3.3}$$

where V_{C2} is the average voltage across C_2 and $\overline{I_{Lb}}$ is the average input/FC current.

At the end of this mode the current through the bridge switches are equal to $0.5\overline{I_{Lb}}$.

Mode T_3: As shown in Fig. 3.3c, S_1~S_4 are turned on and voltage-doubler capacitors C_1 and C_2 will sustain the output power (P_o) . The bridge switches will share the input current $\overline{I_{Lb}}$, and V_{Sc} is equal to V_{ca} as defined in Mode 1. The primary current and the secondary current are both equal to zero. During T_1-T_3 periods the input current i_{Lb} increases linearly as:

$$i_{Lb}(t) = i_{Lb}(t_1) + \frac{V_{fc}}{L_b}(t - t_2) \tag{3.4}$$

During these periods the voltage across the voltage-doubler rectifier diodes is equal to $V_o/2$

Mode T_4: At t_3, S_3 and S_4 are turned off and half of the input current charges the C_{p3} and C_{p4} respectively to v_{Ca} at t_4. As shown in Fig. 3.3d, due to discharge of C_{pc} the clamp switch voltage drops to zero and C_a is charged to v_{Ca}. At this instant, C_{p3} and C_{p4} are fully charged. Then, the bridge and clamp switch voltages can be described using the following steady-state equations:

$$v_{AB}(t) = v_{Cp3,4}(t) = v_{Ca}(t - t_3) \tag{3.5}$$

$$v_{Sc}(t) = V_{Ca} - v_{Ca}(t - t_3) \tag{3.6}$$

Mode T_5: When one pair of diagonal bridge switches is turned off, the input current i_{Lb} tries to commutate to the transformer primary, which leads to a rapid rise in the voltage across the bridge due to the presence of the transformer leakage inductance L_σ. As soon as the voltage across the bridge is greater than the reflected secondary voltage (V'_{sec}), the anti-parallel diode of the clamp switch starts to conduct and the input current diverting to the clamp capacitor, as depicted in Fig. 3.3e. Hence, the voltage across the bridge is clamped to the clamp capacitor voltage (v_{Ca}).

At t_4, the current through the clamp circuit (i_{Ca}) will be equal to the $\overline{I_{Lb}}$. The steady-state equations of $i_{L\sigma}$ and v_{Ca} can be written as follows:

$$i_{L\sigma}(t) = \overline{I_{Lb}}(1 - \cos\omega_o(t - t_4)) \tag{3.7}$$

$$v_{Ca}(t) = V_{Ca} + \overline{I_{Lb}} Z_o \sin(\omega_o (t - t_4)) \tag{3.8}$$

where the resonant frequency ω_o and the resonant impedance are given as:

$$\omega_o = \frac{1}{\sqrt{L_\sigma C_a}}, \quad \text{and} \quad Z_o = \sqrt{\frac{L_\sigma}{C_a}} \tag{3.9}$$

Resonance takes place between L_σ and C_a until $t = t_7$.

Mode T_6: As shown in Fig. 3.3f, S_c will be turned on before the clamp capacitor start to discharge its energy. As the capacitor voltage slowly increases, the primary current $i_{L\sigma}$ rises gradually from zero at t_4 until its equal to the input current $\overline{I_{Lb}}$ at t_6. At the same time the capacitor current declines from $\overline{I_{Lb}}$ to zero. This mode ends when i_{Ca} drops to zero, giving the peak voltage across the bridge switches as:

$$V_{Ca,max} = \sqrt{\frac{L_\sigma}{C_a}} \overline{I_{Lb}} + \frac{V_{c1}}{n} \tag{3.10}$$

Mode T_7: Due to the resonance between C_a and L_σ the capacitor discharges again through S_c, which takes $i_{L\sigma}$ above the value of $\overline{I_{Lb}}$. At t_7, the currents in S_1, S_2 and L_σ are equal to two times the input current $\overline{I_{Lb}}$. The equivalent circuit of this mode is depicted in Fig. 3.3g.

During the off period of the one of the diagonal bridge switches the input current decreases linearly as:

$$i_{Lb}(t) = i_{Lb}(t_3) + \frac{V_{fc} - V_{Ca}}{L_b}(t - t_3) \tag{3.11}$$

While the primary current increase as given in (3.7).

Mode T_8: At t_7, S_c is turned off while S_1 and S_2 remain on and S_3 and S_4 are turned off; C_{pc} is charging into V_{Ca} but C_{p3} and C_{p4} are discharging. Here, $i_{L\sigma}$ is still greater than $\overline{I_{Lb}}$. At t_8 the current via S_1 and S_2 start to decline until reaches equal to $\overline{I_{Lb}}$ at t_9. This mode is indicated in Fig. 3.3h. At the end of this mode D_1 turned-off with zero current. During modes T_7 and T_8 the current via S_1 and S_2 is greater than i_{Lb} and equal to:

$$i_{S1-2}(t) = i_{Lb}(t) + i_{Ca}(t) \tag{3.12}$$

3.2.2 DC/DC Voltage Conversion ratio

When the power transfers to the output during Mode T_5, the converter high voltage side (HVS) can be represented by the equivalent circuit shown in Fig. 3.4[4].

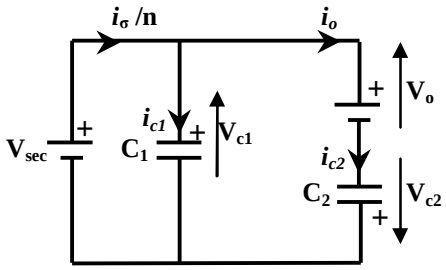


Fig. 3.4 Equivalent circuit diagram of the converter during mode T_5

According to the Kirchhoff's voltage law, the voltage across C_1 is equal to:

$$v_{C1}(t) = V_o - v_{C2}(t) \tag{3.13}$$

If the output capacitors C_1 and C_2 are designed as large enough, then

$$v_{C1}(t) = V_{C1} \quad \text{and} \quad v_{C2}(t) = V_{C2} \tag{3.14}$$

[4]The power transfers to the output only when a pair of bridge diagonal bridge switches is switched off.

where $v_{C1}(t)$, $v_{C2}(t)$, V_{C1}, and V_{C2} are the instantaneous and average voltage across the capacitors C_1 and C_2 respectively.

By substituting the above condition in (3.13), the voltages V_{C1}, V_{C2}, and V_{sec} are always equal to half of the DC output voltage V_o. Consequently, the amplitude of the reflected secondary voltage $v'_{sec}(t)$ will be equal to $V_o/2n$. The voltage across the primary windings $v_{pri}(t)$ is clamped by the average clamp capacitor voltage V_{Ca}. Thus, the reflected secondary voltage $v'_{sec}(t)$ during the first half-cycle (T_4-T_9) can be represented as:

$$v'_{sec}(t) = V_{Ca} = \frac{V_o}{2n} \tag{3.15}$$

By applying the volt-second balance principles across the L_b during one switching cycle (see Fig. 3.2) the relation between V_{fc} and the clamp capacitor voltage V_{ca} can be written as:

$$V_{fc}d_1 + (V_{fc} - V_{Ca})d'_1 + V_{fc}d_2 + (V_{fc} - V_{Ca})d'_2 = 0 \tag{3.16}$$

According to the timing diagram in Fig. 3.2, the steady-state values of the duty cycles D and D' are given respectively by[5]:

$$D = \frac{d_1 + d_2}{2} \tag{3.17}$$

and

$$D' = \frac{d'_1 + d'_2}{2} \tag{3.18}$$

where D' is complementary duty cycle equal to (1-D)

[5] D and D' include the conduction period of the MOSFETs anti-parallel diode and the time intervals for charging and discharging parasitic capacitances

Substituting (3.17) and (3.18) in (3.16), the relationship between the average clamp capacitor voltage and the average FC voltage found to be:

$$V_{Ca} = \frac{V_{fc}}{D'} \tag{3.19}$$

Substituting (3.19) in (3.15), the converter's voltage conversion ratio (M) can be derived as:

$$M = \frac{V_o}{V_{fc}} = \frac{2n}{(1-D)} \tag{3.20}$$

(3.20) shows that the voltage conversion ratio is related to the transformer turns ratio n and the duty cycle D only. Hence, if n = 7.4 (see Section 3.3 for more details on the transformer design) and M = 25[6], then the maximum required duty cycle (D_{max}) is equal to 0.41.

It should be noted that, (3.20) is a simple representation of the converter's voltage conversion ratio. It ignores the non-effective duty cycle of the switches due to the presence of parasitic elements and load resistance. Therefore, the voltage conversion ratio in (3.20) is re-evaluated in this section as described below.

Based on the assumptions (7) and (8) in Section 3.2.1, a plot of the absolute values of the voltage-doubler capacitor currents $|i_{C1}|$ and $|i_{C2}|$, the output current i_o, voltage-doubler diode currents i_{D1} and i_{D2}, and the primary current $|i_{L\sigma}|$ during one cycle is shown in Fig. 3.5.

[6] The required M at the minimum FC voltage (26V) is equal to 25 if the output voltage V_o is equal to 650V.

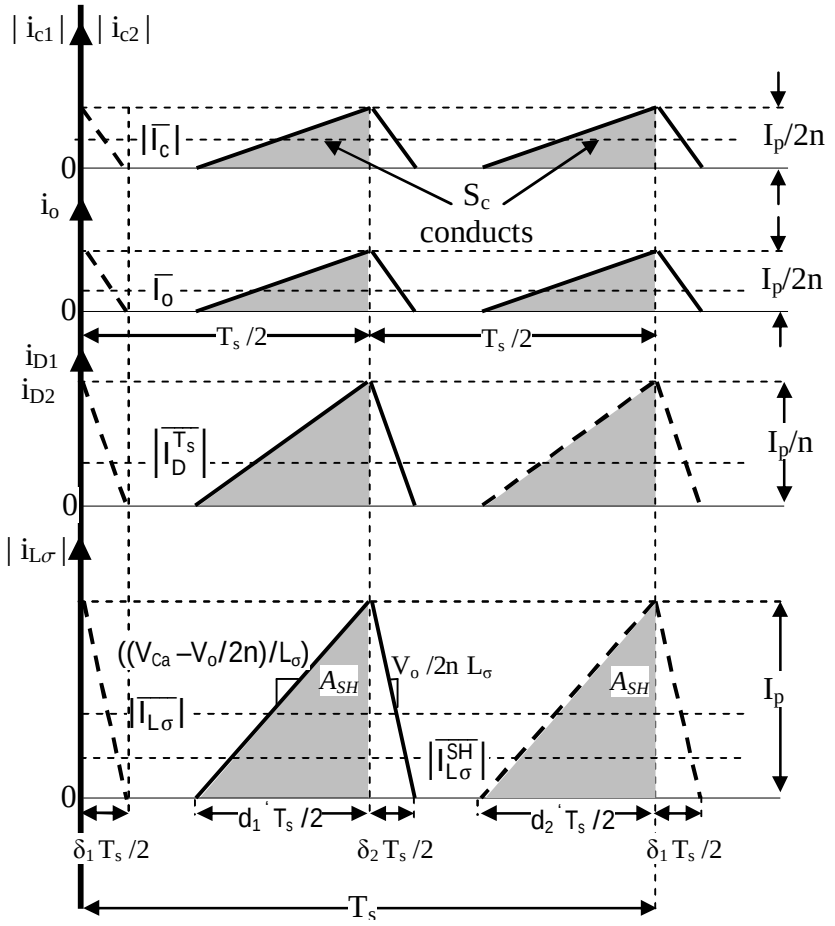


Fig. 3.5 Waveforms of the absolute values of the currents through the output capacitors C_1 and C_2 and primary winding, and the currents through the output resistor R_o and rectifier diodes D_1 or D_2

The absolute values have been taken for the primary and voltage-doubler capacitor currents to represent the correlation between the instantaneous values of $i_{L\sigma}$ and i_{C1}/i_{C2} and the DC output current i_o. The shaded area under the current waveforms indicates the charging and discharging periods of the clamp capacitor C_a.

According to the converter operation (see Fig. 3.3), during the modes T_5-T_8 and T_9-T_{10}[7] the expression of the primary current $i_{L\sigma}$ can be given as

[7] Notice that modes T_9-T_{10} are similar to modes T_1-T_2

$$i_{L_\sigma}(t) = \begin{cases} \dfrac{V_{Ca} - V_o/2n}{L_\sigma}(t - t_4), & t_4 \le t \le t_7 \\ \dfrac{-V_o/2n}{L_\sigma}(t - t_7) + i_{Lt}(t_7), & t_7 \le t \le t_{10} \end{cases} \tag{3.21}$$

The average of the absolute value of the primary current $|\overline{I_{L\sigma}}|$ can be described as:

$$|\overline{I_{L\sigma}}| = \frac{1}{2} I_p (D' + \Delta) \tag{3.22}$$

where D' is defined in (3.18), I_p is the peak current in the primary side which is equal to twice the average input current $\overline{I_{Lb}}$ (see Mode T_7 and Fig. 3.3g) , and Δ is the steady-state duty cycle which represents the fraction of the period during which energy is transferred from the leakage inductance L_σ to the secondary side and is equal to:

$$\Delta = \frac{\delta_1 + \delta_2}{2} \tag{3.23}$$

During the operation modes T_1-T_2 and T_5-T_8 for the first half-cycle (see Fig. 3.3), both the charging current of C_1 and discharging current of C_2 (or vice versa) flow through the diodes D_1 or D_2. Thus, the average current $\overline{I_{D1}^{Ts/2}}$ and $\overline{I_{D2}^{Ts/2}}$, via the diodes D_1 or D_2, is equal to twice the absolute value of the average of the currents i_{C1} and i_{C2} during the half cycle $T_s/2$, i.e. $\overline{|I_{C1}^{Ts/2}|}$ or $\overline{|I_{C2}^{Ts/2}|}$ (see Fig. 3.5). The absolute value of the average of the currents i_{C1} and i_{C2} during one cycle T_s are equal to the average output current $\overline{I_o}$, i.e. $|\overline{I_{C1}^{Ts}}|$ and $\overline{|I_{C2}^{Ts}|}$. Hence, the average of the absolute secondary current $|\overline{I_{L\sigma}}|/n$ is equal to twice the average output current $\overline{I_o}$ during one cycle T_s. Consequently, the average of the primary current$|\overline{I_{L\sigma}}|$ is equal to $(2n\overline{I_o})$, where $\overline{I_o}$ equal to

$$\overline{I_o} = \frac{V_o}{R_o} = \frac{\overline{I_{Lb}}}{2n} D' \qquad (3.24)^8$$

Using (3.24), (3.22) can be re-written as:

$$2n\frac{V_o}{R_o} = \frac{1}{2} I_p (D' + \Delta) \qquad (3.25)$$

As shown in Fig. 3.2 (at the time $t = t_4$), the primary current $i_{L\sigma}$ is remains equal to zero until the clamp capacitor current i_{Ca} is less than the average input current $\overline{I_{Lb}}$. During the period $d_1'/2$ or $d_2'/2$ of each half-cycle, while the clamp switch conducts, the primary current increases with a slope of $((V_{ca} - V_o/2n)/L_\sigma)$ (see (3.21) and assumptions (7) and (8) in Section 3.2.1). At the end of this period, the primary current attains the peak value I_p given by:

$$I_p = \left(\frac{V_{ca} - \frac{V_o}{2n}}{L_\sigma} \right) D' T_s \qquad (3.26)$$

Similarly, during the period $\delta_1/2$ or $\delta_2/2$ of each half cycle, the primary current decreases with a slope equal to $(V_o/2nL_\sigma)$. This interval ends when the voltage-doubler diodes become reverse biased (see Fig. 3.3c & d).

By applying the volt-second balance principle across the L_σ during one switching cycle, the following relation can be obtained:

$$\left(V_{ca} - \frac{V_o}{2n} \right) D' - \left(\frac{V_o}{2n} \right) \Delta = 0 \qquad (3.27)$$

From (3.27), the duty cycle Δ is found as:

---

[8] If $P_o = P_{in}$ then $V_{fc}\overline{I_{Lb}} = V_o I_o$ substitution this condition in (3.20) then the right term of (3.24) can be obtained.

$$\Delta = \frac{2nD'}{V_o}\left(V_{Ca} - \frac{V_o}{2n}\right) \tag{3.28}$$

Substitution of (3.26) and (3.28) in (3.25) finally yields for the true voltage conversion ratio of the converter

$$M = \frac{\sqrt{R_o T_s}\sqrt{32L_\sigma n^2 + D'^2 T_s R_o} - D'T_s R_o}{8L_\sigma n} \tag{3.29}$$

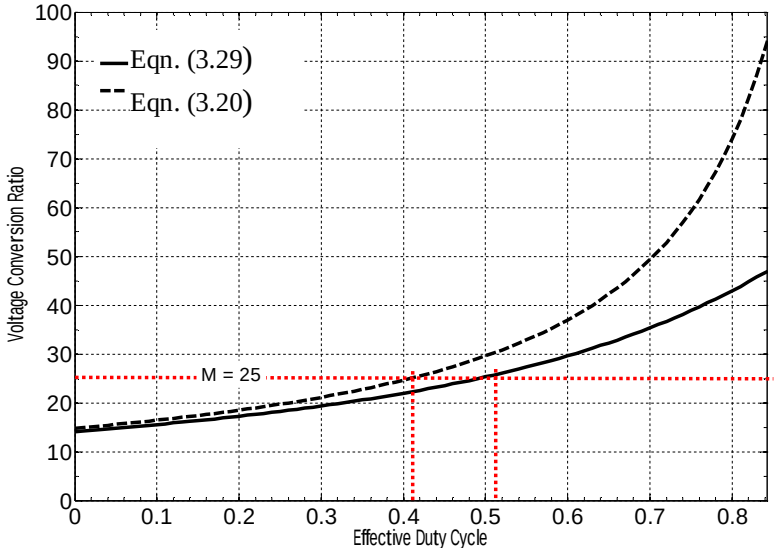


Fig. 3.6 Converter's voltage conversion ratio versus effective duty cycle

From (3.29), it can be noted that the converter's conversion ratio depends on the leakage inductance L_σ, the switching frequency f_s, and the load resistance R_o in addition to the transformer turns ratio n and duty cycle D. This means that these parameters must be adjusted together to obtain the required voltage conversion ratio M.

Fig. 3.6 shows the difference in voltage conversion ratio obtained from (3.20) and (3.29) against the effective duty cycle D using the following parameters: V_{fc}=26V,

L_σ=2μH[9], n=7.4, f_s=20kHz, R_o=352Ω. For the same M, it can be noted that the presence of L_σ causes a loss of regulation range (i.e. the DC link voltage V_o cannot reach to the required level). This loss of regulation can be attributed to the non-effective duty cycle D_{loss}, defined as

$$D_{loss} = \frac{4nV_oL_\sigma}{T_sR_oV_{fc}} \tag{3.30}$$

As indicated in Fig. 3.6, it is obvious that D_{loss} increases as the effective duty cycle D increases resulting in an increased loss of regulation at higher D. For example, at M=25 and D = 0.42 the loss of regulation range is about 3.

3.2.3 Soft-Switching Range

In this section an analysis of the converter operation under soft switching conditions of the primary switches and the voltage-doubler rectifier diodes is presented.

As shown in Fig. 3.3 and Fig. 3.2, the active-clamp circuit can realize ZVS for the bridge switches at turn-on by turning off S_c before the other pair of diagonal switches is turned on. This halts the discharge of C_a, and the deficit between the transformer current and the input current will discharge the parasitic capacitances C_{p1}~C_{p4} of the bridge switches, resulting in conduction of their anti-parallel diodes, thus reducing the voltage across the bridge switches to zero before they are turned on. To ensure ZVS of the bridge switches at the turn-on, the required dead time T_{dead1} between the bridge switches

[9]An estimation test has been done to accurately estimate the leakage inductance L_σ value. This has been done by measuring the voltage stress across the bridge switching at the full load (without active clamp circuit) and then selecting the leakage inductance value in PSpice that gives the same overshoot voltage across the bridge switches that obtained from the measured results. A B-H curve experiment has been done in the Laboratory on the transformer by applying 20 kHz square waveform from 60V power amplifier to measure the leakage inductance. Due to the saturation of the power amplifier after 60V the maximum voltage that can be obtained on the secondary side is limited to 450V with n=7.4. Thus, the transformer is under low flux operation. Hence, the measured leakage inductance value which found equals 4.43μH.

and the clamp switch S_c should not exceed the full Resonant period between C_{p3}~C_{p4}, C_{pc} and L_σ (see Section 3.3.3), i.e.

$$T_{dead1} = 2\pi\sqrt{(C_{p3} + C_{p4} + C_{pc})L_\sigma} \tag{3.31}$$

with $C_{p3} = C_{p4} = 16nF$[10], $C_{pc}=10nF$[11] and $L_\sigma = 2\mu H$, this yeilds $T_{dead1} \cong 1.8\mu sec$[12]

Unfortunately, the bridge switches operate in the hard-switching (HSW) mode at turn-off. However, the turn-off loss is not high since the bridge switches are operating with low voltages (only 44V for the proposed converter compared to 74V for Config.3 and around 200V for the Config.1 (see Section 3.4)).

In the case of the clamp switch S_c, as soon as the voltage across the bridge switches is greater than the reflected secondary voltage V'_{sec}, the anti-parallel diode of S_c starts to conduct. Hence, the clamp switch can be turned on with ZVS. As shown in Mode T_5, the required dead time T_{dead2} between the turn-off of one pair of the diagonal bridge switches and the turn-on of the clamp switch should be of sufficient interval to discharge C_{pc} and charging C_{p3}~C_{p4} with half the input current to ensure ZVS at the turn-on of the S_c. This dead time can be calculated from (3.31).

If the resonant frequency f_o between the transformer leakage inductance L_σ and the clamp capacitance C_a has been designed appropriately in relation to the switching frequency f_s (see Section 3.3.2) the clamp switch can be turned off with near-ZCS (see Fig. 3.32). The proposed approach described in Section 3.3.2 also allows the voltage-doubler rectifier diodes to turn on with zero current by slowing down the rise of the clamp capacitor current i_{ca} (see Fig. 3.34). Since the output current is discontinuous the

[10] These values are obtained from the datasheet of SKM120B020 MOSFET device.
[11] This value is obtained from the datasheet of IXFN73N30MOSFET device.
[12] This value is set in the DSP as shown in Appendix H.

voltage-doubler diodes are operating under ZCS when the diodes D_1 and D_2 turn off. Hence, the proposed converter in combination with the proposed optimum design of the active clamp circuit (see Section 3.3.2) results in ZCS turn-off and turn-on for the rectifier diodes.

Table 3.1 summarises the switching modes of the MOSFET's and diodes of the proposed converter.

TABLE 3.1
SWITCHING MODES OF THE MOSFET'S AND DIODES OF THE PROPOSED CONVERTER

Switching Instant	S_1~S_4	S_c	D_1~D_2
Turn-off	HSW	Near-ZCS	ZCS
Turn-on	ZVS	ZVS	ZCS

3.2.4 Input Current Ripple

As described in Section 2.2, the FC generator is characterised by a low output voltage and a high output current, and has a strict current ripple requirement. For that reason, a CFC topology is preferred for FC applications, as mentioned in Section 2.5.1.

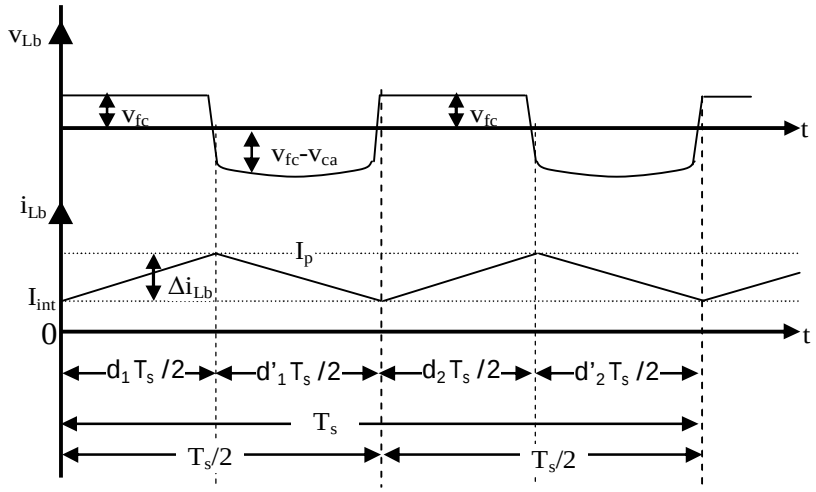


Fig. 3.7 Voltage and current waveforms of the boost inductor

Fig. 3.7 shows the waveforms of the boost inductor voltage v_{Lb} and current i_{Lb}, where it can be seen that the input current rises during the overlap periods $d_1T_s/2$ and $d_2T_s/2$ then falls during the off periods, $d_1'T_s/2$ or $d_2'T_s/2$, of each pair of diagonal switches respectively. Hence, the frequency of the input current ripple (Δi_{Lb}) is twice the switching frequency $2f_s$ ($f_s=1/T_s$) and it can be obtained as:

$$\Delta i_{Lb} = I_p - I_{int} = \frac{V_{fc}}{L_b} DT_s \tag{3.32}$$

where D is defined in (3.17) and I_{int} is the initial value of the input current as indicated in Fig. 3.7.

By substituting (3.20) in (3.32), the input current ripple Δi_{Lb} in relation to the output voltage is obtained as:

$$\Delta i_{Lb} = \frac{V_o}{2nL_b}(1-D)DT_s \tag{3.33}$$

Using the same steps as above the input current ripple Δi_{Lb_conv} of the conventional active clamp FBCFC in Config.3 can be derived as:

$$\Delta i_{Lbconv} = \frac{V_o}{nL_b}(1-D)DT_s \tag{3.34}$$

It is obvious from the two equations above that the proposed converter exhibits a current ripple that is half of that of the Config.3 for the same DC link voltage, which will have a positive effect on the FC lifetime. Consequently, for the same ripple current the proposed converter can be designed with a lower boost inductance.

3.3 Further Efficiency Improvements and Design Considerations

This section introduces a number of steps that have been taken in the design of the proposed converter in order to further improve the efficiency. The proposed approaches address the important parameters that affect the performance of the FC converter, such as input current ripple, voltage rating of the converter's switches, the effect of parasitic elements and EMI problems.

3.3.1 Analysis and Remedies of Effects of the Parasitic Elements

3.3.1.1 Existing FBCFC Set-Up

At the start of the investigations, an experimental set-up of a DC-DC boost converter with start-up flyback converter circuit already existed, built by John Gow as detailed in [79]. The schematic diagram of this converter is shown in Fig. 2.30 and the converter prototype shown in Fig. 3.8. Based on this converter prototype, the proposed converter has been developed and evaluated.

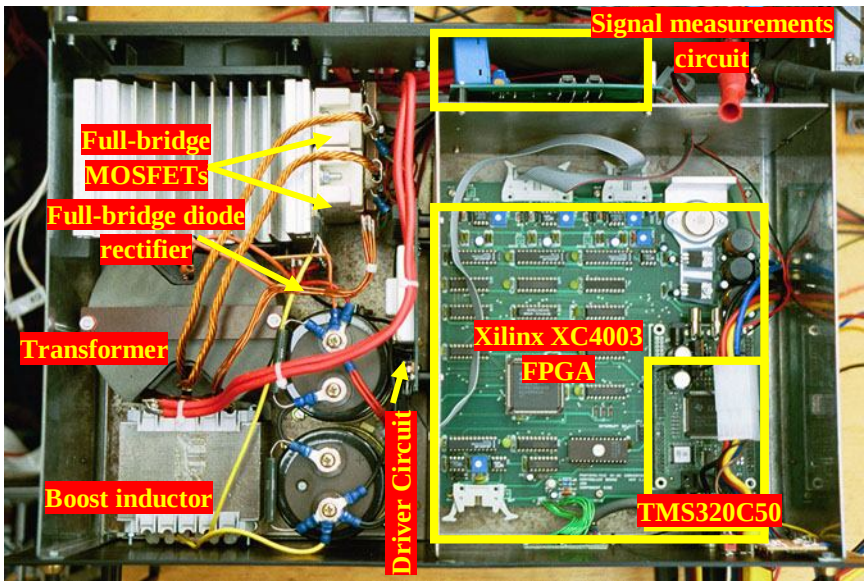


Fig. 3.8 Prototype of the CFC built by John Gow in [79]

Although the proposed FC converter has shown promising features, such as a lower component voltage-rating, higher voltage conversion ratio, and lower current ripple, a problem in establishing a hardware implementation is caused by the parasitic elements of the converter devices. It was noted that these elements generated a high frequency ringing resulting in a considerable increase in switching losses, voltage stress, current stress, and EMI radiated noise through the converter. This prototype converter was also used by a previous student, who when faced with the same problem was forced to use a slower sampling time and lower bandwidth for the control system [10]. To solve this problem further theoretical and modelling analysis has been developed on the converter circuit included different parasitic elements to accurately assess the converter performance. Based on this analysis some modifications have been developed to improve the performance of the converter.

3.3.1.2 Impact of the Parasitic Elements on the Converter Performance

i- Detailed Analysis of the Effect Parasitic Elements

Based on simulation and hardware implementation, it was found that the most significant parasitic elements that have the biggest impact on the converter performance include the stray inductances of the switching devices, the stray capacitances of the boost inductor and transformer, and the parasitic capacitance of the rectifier diodes. These elements are included in the detailed converter circuit shown in Fig. 3.9 [13.] The most significant interactions between these elements occur during the overlap period $d_1T_s/2$ and/or $d_2T_s/2$ of the bridge switches.

[13] Notice that the analysis does not consider the effect of stray inductances of the connection wires.

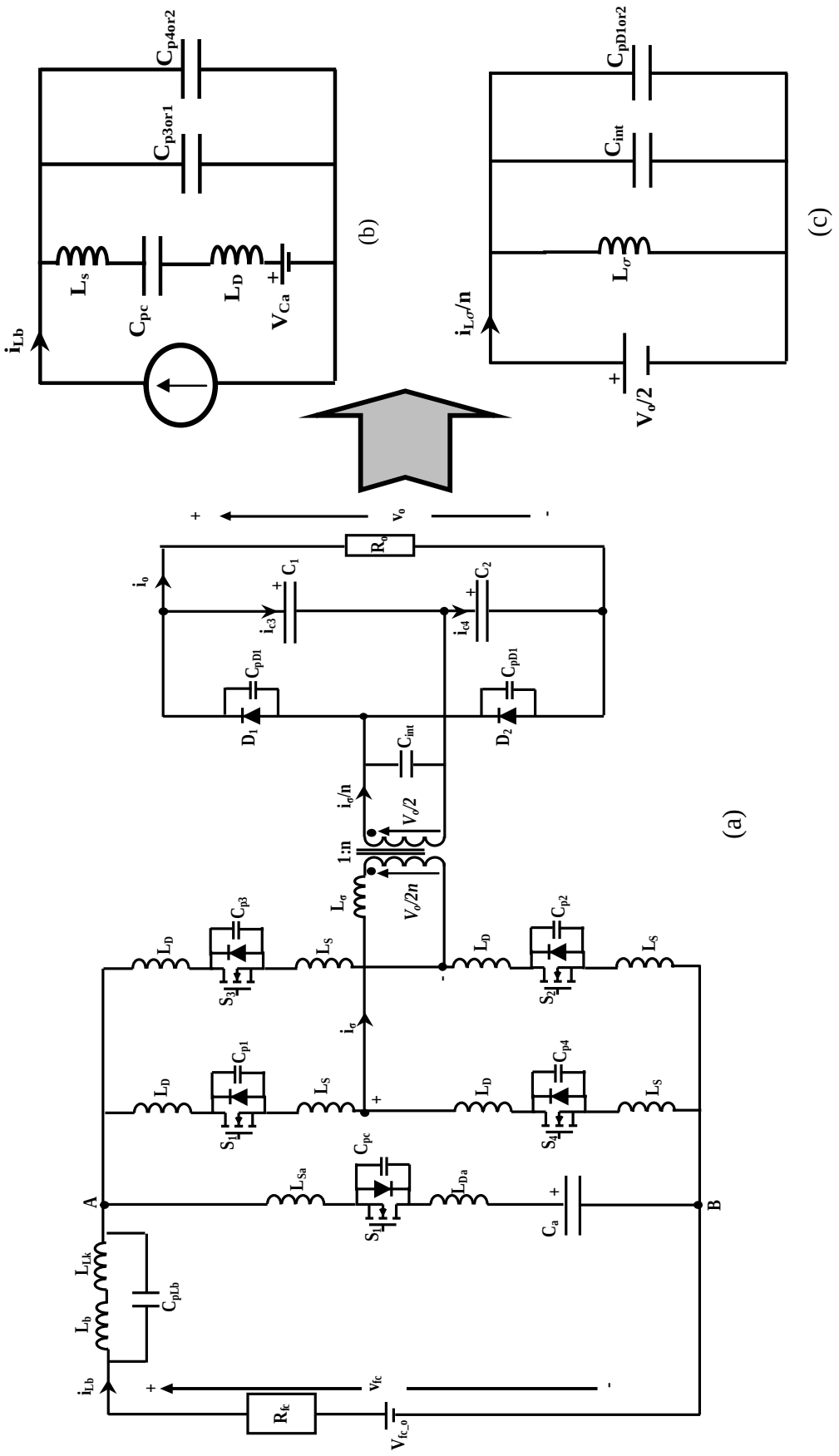


Fig. 3.9 (a) Circuit diagram of the proposed converter including the parasitic elements, (b) equivalent circuit of the LVS when the clamp switch is turned off, and (c) equivalent circuit of the HVS when the diodes turns off.

As indicated in Fig. 3.9, the interactions between these parasitic elements during the overlap period can be described using the two equivalent resonant circuits depicted in Fig. 3.9b and c respectively. These circuits are denoted as “Resonant Circuit I” and “Resonant Circuit II” and are described below.

Resonant Circuit I (Fig. 3.9b)*:* at the start of the overlap period $d_1T_s/2$ and/or $d_2T_s/2$, where all the bridge switches S_1~S_4 are beginning to turn on and the clamp switch S_c is starting to turn off, the stray inductances L_D+L_S of the clamp switch tends to resonate with the parasitic capacitance C_{pc} and the parasitic capacitances of the diagonal switches (i.e. C_{p3or1} and C_{p4or2}). The resonant frequency f_{r1} of this circuit is equal to

$$f_{r1} = \frac{1}{2 \times \pi \times \sqrt{(L_D + L_S) \times \frac{(C_{p3or1} + C_{p4or2})C_{pc}}{C_{pc} + C_{p3or1} + C_{p4or2}}}} \tag{3.35}$$

Using the datasheets of the clamp switch (IXFN73N30) and the bridge switches (SKM120B020) the parameters of (3.35) can be obtained as C_{p3or1} = C_{p4or2} = 16nF, C_{pc}=10nF, and L_D+L_S =30nH. Then, the ringing frequency caused by “Resonant Circuit I” is up to $f_{r1} \cong$ 7.5MHz.

The energy stored in the stray inductances (L_D+L_S) of the clamp switch will dissipate in S_c during device turn-off. Thus, soft-switching of the clamp switch S_c at turn-off cannot be achieved, resulting in a higher switching loss. This energy (E_{SW_off}) is given as:

$$E_{SW\_off} = \frac{I_S^2(L_D + L_S)V_{Sc\_pk}}{2(V_{Sc\_pk} - V_{ca})} \tag{3.36}$$

where V_{Sc_pk} is the peak voltage of the switch S_c and I_S is the RMS MOSFET current. The parameters L_D+L_S, V_{Sc_pk}, and V_{Ca} are obtained from the MOSFET IXFK73N300 data sheet and calculations as 30nH, 300V, and 44V (see (3.15)) respectively.

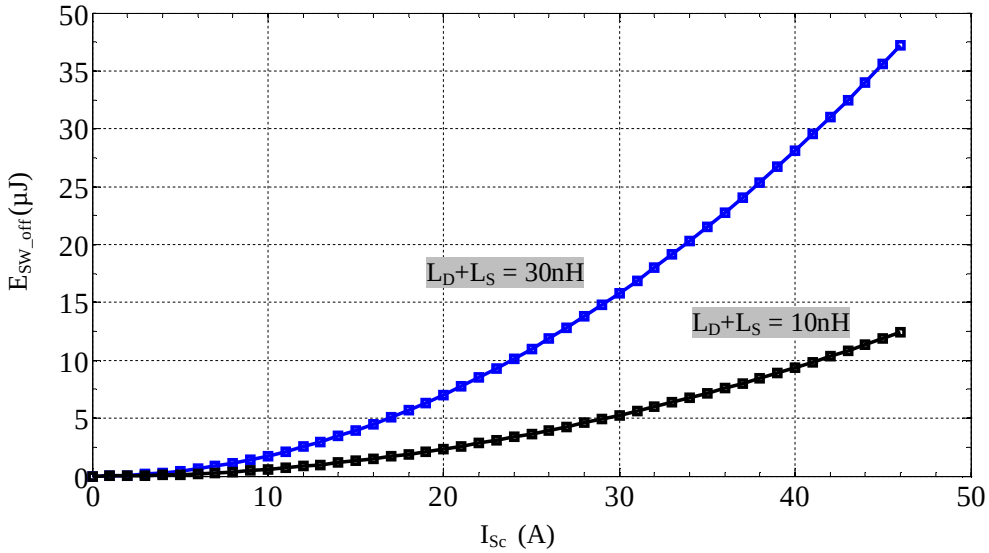


Fig. 3.10 Dissipated energy in the clamp switch S_c during the turn-off period due to resonant in "Resonant Circuit I"

Fig. 3.10 shows the switching loss in the clamp switch at turn-off due to the parasitic elements of the "Resonant Circuit I" for two values of L_D+L_S. It is obvious from Fig. 3.10 that the circulation energy E_{SW_off} increases with the required load and it can be decreased only by using switching devices with a lower stray inductance[14] (see black line in Fig. 3.10).

The ringing caused by the "Resonant Circuit I" has another impact on the converter components as described in the next section.

Resonant Circuit II (Fig. 3.9c): once the period $\delta_1 T_s/2$ and/or $\delta_2 T_s/2$ is completed, a second ringing occurs between the inherent capacitance (C_{pD1or2}) of the non-conducting rectifier diodes D_1 and D_2, inter-winding capacitance (C_{int}) of the transformer and the

[14] For the calculation and simulation analysis the stray inductance of the wires is neglected. However, in practice these parameters are lumped together with the stray inductances of the switch resulting in increased switching loss and alteration the frequency of oscillation.

leakage inductance $L_{\sigma 2}$ of the secondary windings, as clarified in Fig. 3.9c. The resonant frequency f_{r2} due to this Resonant circuit can be found as

$$f_{r2} = \frac{1}{2 \times \pi \times \sqrt{L_{\sigma 2} \times (C_{pD1or2} + C_{int})}} \quad (3.37)$$

Since "Resonant Circuit II" incorporates $L_{\sigma 2}$ with a higher inductance than in circuit I, this circuit is expected to be ringing at a lower frequency.

When the rectifier diodes turn off at the end of the period $\delta_1 T_s/2$ and/or $\delta_2 T_s/2$, the resonance causes a high voltage stress across the rectifier diodes and the energy stored in the capacitances C_{pD1or2} and C_{int} will be dissipated in the rectifier diodes and the secondary winding. This ringing continues through the period $((d_1 - \delta_1)T_s/2)$.

However, in the actual converter this loss of regulation increased further and therefore the maximum duty cycle D_{max} has been selected around 0.6.

ii- Validation of Analysis

To validate the previous theoretical analyses, parasitic elements were included in the PSpice model as described in Section A below. After this the PSpice model has been verified by experimental results as described in Section B.

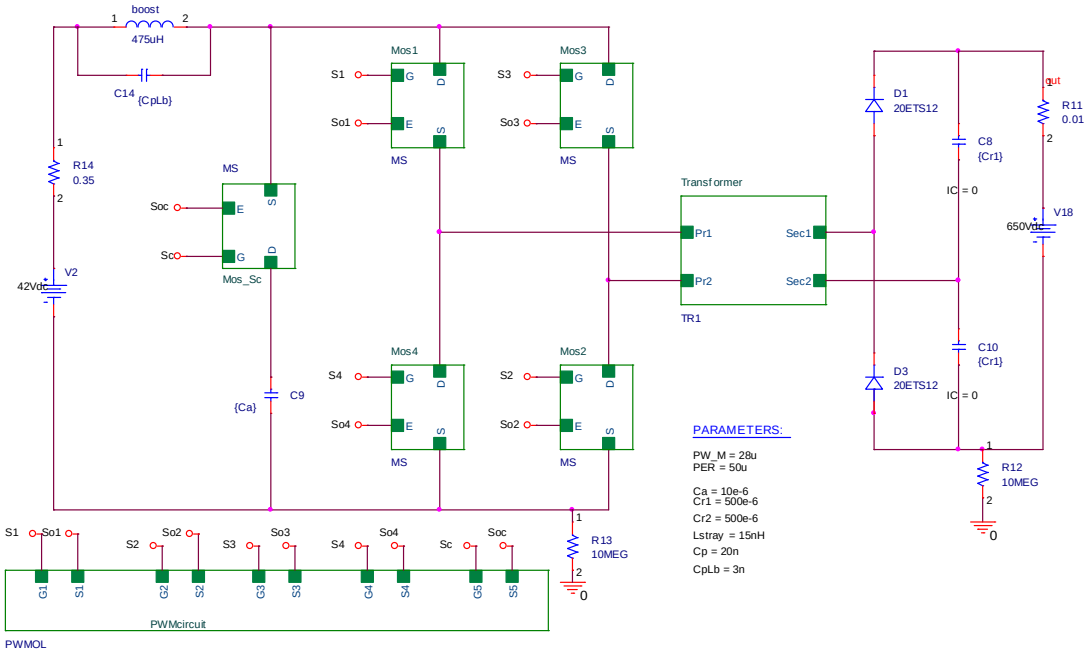
The parameters and components that have been used for the simulation and measured results are given in Table 3.2.

TABLE 3.2
PARAMETERS AND COMPONENTS OF THE CONVERTER USED FOR THE SIMULATION AND PRACTICAL TESTS

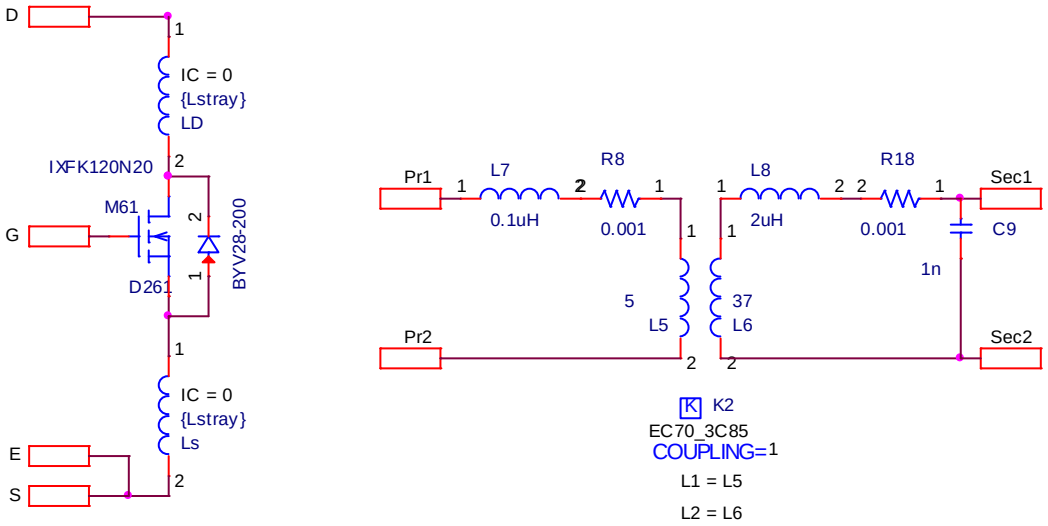
Parameters and Components	**Part/Value Simulation**	**Part/Value Practical**
Power Rated	1.2kW	1.2kW
Leakage inductance	2µH	2µH
Output capacitors	2×500µF Polarized capacitors	2× 470µF, 400V Electrolytic + 1uF, 1000V polyester connected in parallel
Clamp capacitor	10µF Polarized capacitor	10µF, 250V polyester
Main switching devices	IXFK120N20 (200V/120A) $R_{DS}(on)$ =17mΩ	SKM120B02 (200V/120A) $R_{DS}(on)$=17mΩ, with SKHI21A Driver
Clamp switch device	IXFK120N20 (200V/120A) $R_{DS}(on)$ =17mΩ	IXFK73N300 (300V/73A): $R_{DS}(on)$=45mΩ, with SKHI21B Driver
Transformer turn ratio	5:37	5:37
Boost inductor	475 µH	475 µH
DC input & output voltage	43V (0A) - 26V (46A) ; 650V	43V (0A) - 26V (46A) ; 650V
Rectifier diodes	20ETS12	C2D05120A

A. PSpice Validation

Fig. 3.11 shows the PSpice model of the converter including the parasitic elements. It is worth mentioning here that the PSpice software is preferred over other software packages, such as PSIM, SABER, PLECS and “SimPowerSystems” Toolbox in Simulink, since PSpice uses accurate models of devices, often supplied by the device manufacturers, which are valid under all conditions, including transients. Reference [102], developed by the author, shows comprehensive details and analysis to illustrate why the PSpice is preferred.



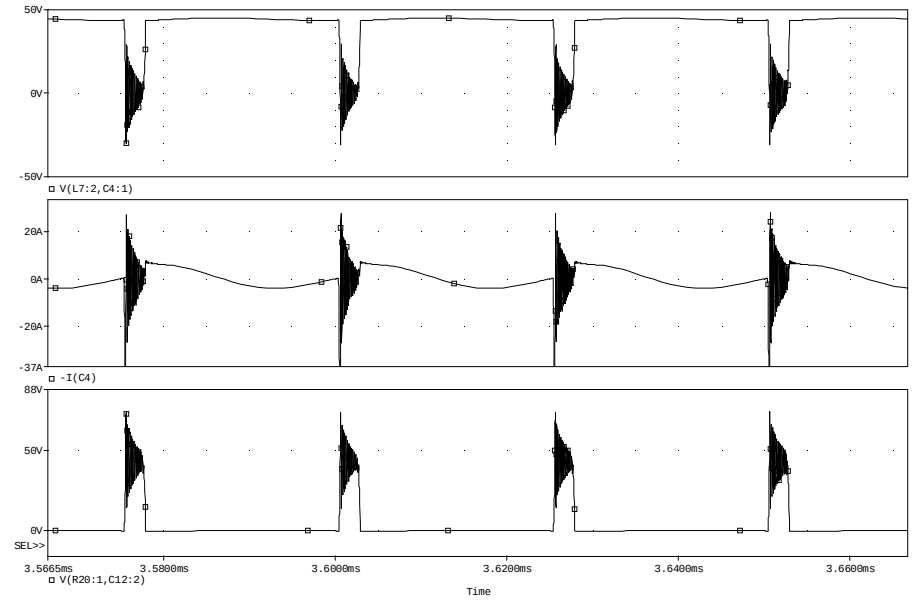
(a)



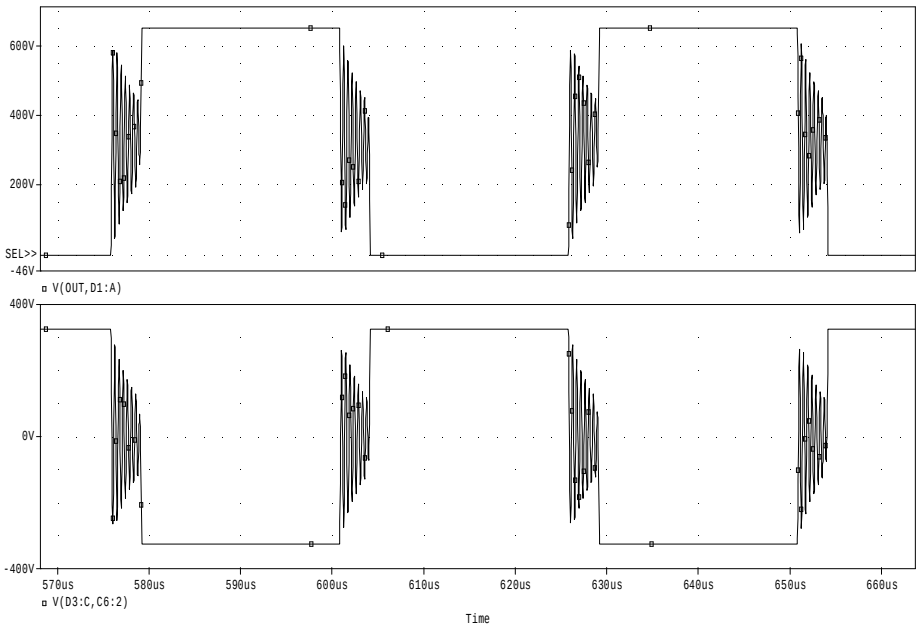
(b) (c)

Fig. 3.11 PSpice schematic diagram of : (a) the proposed converter including the parasitic and stray elements, (b) MOSFET model inside the blocks Mos1~Mos4 and Mos_S_c, and (c) transformer model inside the block TR_1

Simulation results of the bridge voltage v_{AB}, clamp current i_{ca}, and the switch voltage V_{Sc} are shown in Fig. 3.12a.



(a)



(b)

Fig. 3.12 Simulated waveforms showing the effect of the parasitic elements: a) From the top: the bridge voltage, clamp current and clamp switch voltage and b) From the top: voltage across the rectifier diode D_1 and the secondary windings

It can be seen that due to the "Resonant Circuit I" at the start of the overlap period ($d_1T_s/2$ and/or $d_2T_s/2$) a high frequency ringing (up to f_{r1}= 8MHz) is imposed across the clamp switch resulting in a high voltage overshoot. Also, it is obvious that a high

frequency current is generated through the clamp circuit resulting in a peak current greater than $\overline{I_{Lb}}$.

According to Fig. 3.1, the voltage v_{AB} should be equal to zero during the overlap period. However, due to ringing in "Resonant Circuit I", non-zero voltage appears across the bridge switches even when they are turned-on, resulting a higher conduction losses.

Fig. 3.12b shows a lightly damped resonant (2MHz) across the secondary winding and the rectifier diode due to operation of "Resonant Circuit II". It can be seen that these ringing occurs only during the second part of the overlap period $((d_1- \delta_1)T_s/2)$ and $((d_2- \delta_2)T_s/2)$, while during periods $((d'_1+ \delta_2)T_s/2)$ and $((d'_2+ \delta_1)T_s/2)$ the voltage across the rectifier diodes is always clamped by the DC link voltage V_o.

The simulation waveforms confirm the correctness of the theoretical analysis.

B. Practical Validation

The proposed converter was tested based on the layout shown in Fig. 3.8 with a rated power of 1.2kW[15]. The tests were conducted as shown in the schematic block diagram of the experimental set-up of Fig. 3.13. A photograph of the laboratory experimental set-up is shown in Fig. 3.14. The original controller board of the converter in Fig. 3.8 consisting of a TMS320C50 and Xilinx XC4003 FPGA has been replaced with the eZdsp F28x evaluation board. Gating signals (see Fig. 3.15) for the converter switches were generated using this new board, where the overlap PWM algorithm was implemented on the DSP using the TI C2000 Embedded Target software as described in Section 4.6.4 of Chapter 4. The DSP–PWM interface circuit is shown in Appendix B.

[15] Since the Ballard fuel cell module has a rated power of 1.2kW, the converter has been tested for this power level.

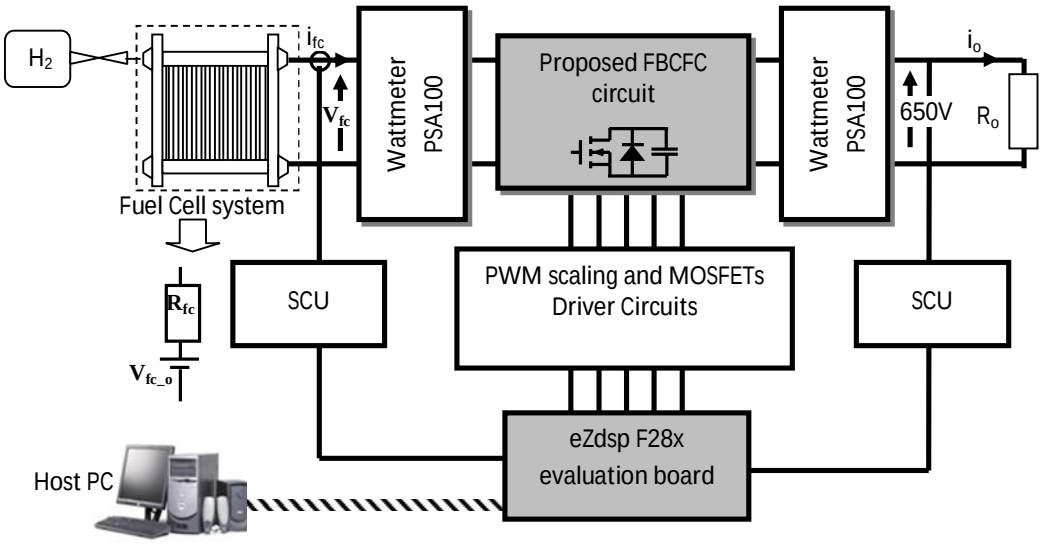


Fig. 3.13 Block diagram of experimental set-up

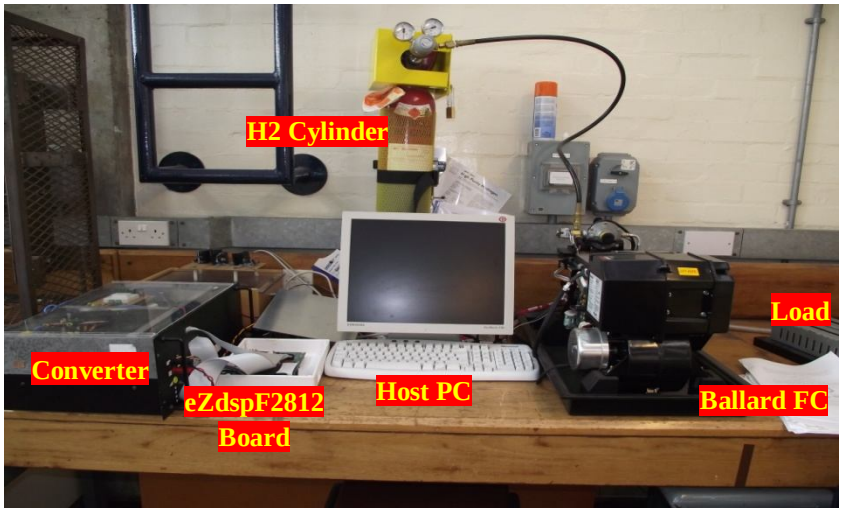


Fig. 3.14 Photograph of the 1.2kW FC power converter experimental set-up

The experimental results are depicted in Fig. 3.16-Fig. 3.19. Fig. 3.16a shows the clamp switch voltage, clamp current, and voltage across the bridge v_{AB}. As predicted by the theoretical analysis the ringing of the clamp voltage and current during the overlap interval is very pronounced. It can also be seen that the voltage across the bridge switches (Fig. 3.16a (ch2)) at the end of the overlap period is well clamped but a ringing occurs at start of the overlap period. This increases the forward voltage across the

MOSFETs. Fig. 3.16b shows that the voltage across the secondary is well clamped to half of the output voltage. But during the overlap period a high frequency ringing (1.7MHz) is imposed across the secondary and across the diodes due to "Resonant Circuit II". The difference in ringing frequency between the practical circuit (1.7MHz) and the PSpice simulation (2MHz Fig. 3.12b) is due to the stray inductance of the wiring.

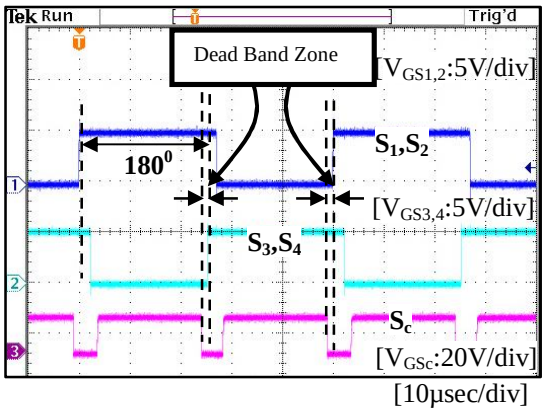


Fig. 3.15 Overlap PWM signals for the bridge and clamp switches

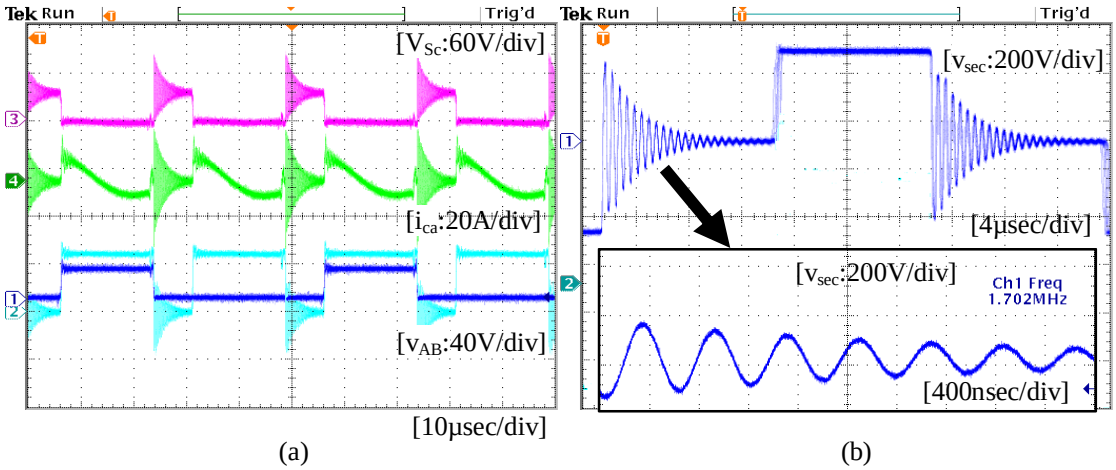


Fig. 3.16 Measured current and voltage waveforms: (a) From top: clamp switch voltage v_{Sc} , clamp current i_{ca} and bridge voltage v_{AB} at 240W, (b) Secondary voltage, v_{sec} with expanded view plot of ringing across the secondary windings

As predicted in the theoretical analysis, Fig. 3.17 shows a simultaneous ringing of the current and voltage of the clamp switch at the turn-off resulting in a high switching loss

due to dissipation of the energy E_{SW_off} through S_c. This loss leads to a reduction of the converter efficiency.

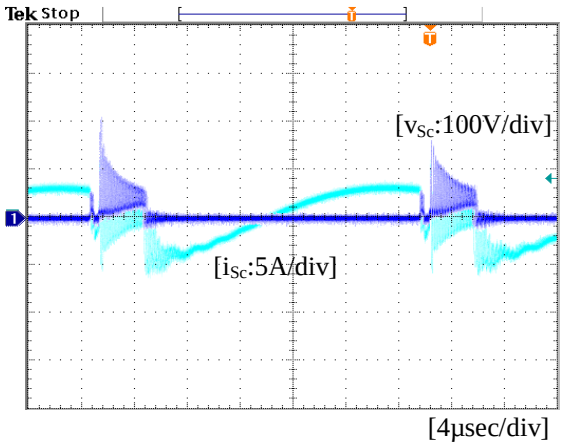


Fig. 3.17 Measured waveforms of the voltage (blue) and current (green) of switch S_c

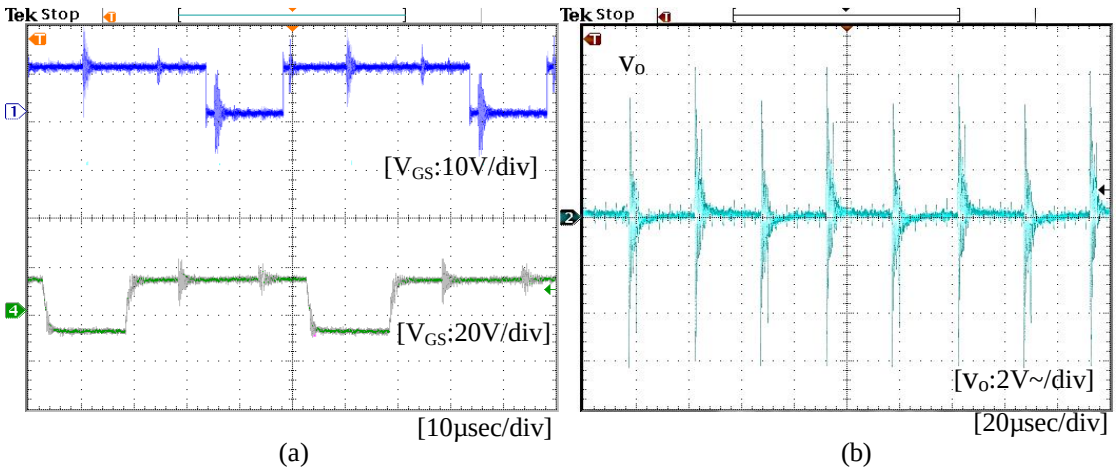
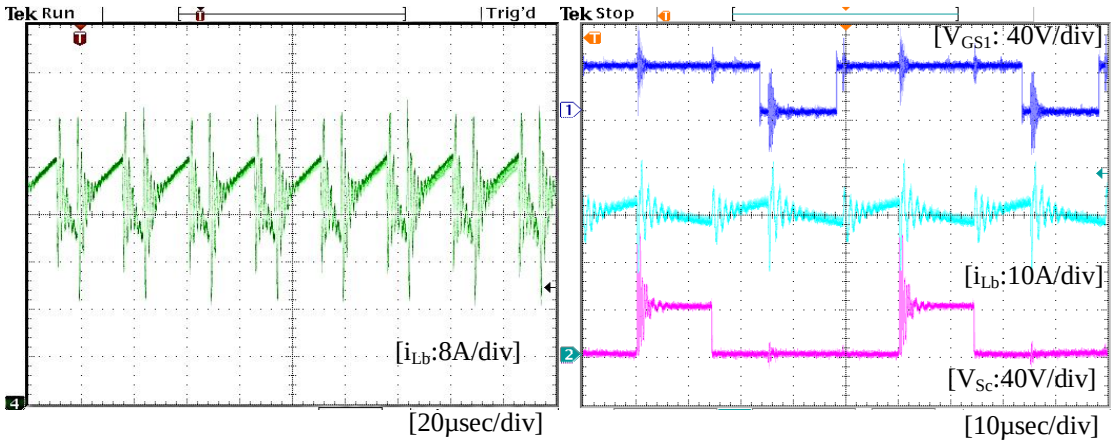


Fig. 3.18 Measured waveforms at 200W of: (a) From the top: Gate signal voltage at the output of the DSP PWM channel and at the output of the MOSFET-drive circuit (ch4), (b) AC output voltage ring.

It was observed in the practical test that the ringing caused by “Resonant Circuit II” on the secondary side also generated a high frequency noise on other waveforms which was not observed in the PSpice model. This high frequency noise is superimposed on the PWM signals that are generated by the DSP, and result in overshoots in the input voltage to the gate driver greater than the permitted voltage (±20V) for the MOSFET, as shown in Fig. 3.18. This leads occasionally to automatic shut-down of the DSP, suppressing the PWM signals. As shown in Fig. 3.18a, this noise also occurs at the

output of the MOSFET-drive circuit. Fig. 3.18b shows the AC output voltage ring caused by “Resonant Circuit II”. In addition, the electrostatic noise caused by that resonant is also coupled with the electronic measurement circuit that is used to scale the FC current and the DC output voltage. In general, the resonant results in serious EMI emanating from the converter and must be attenuated.



(a) (b)

Fig. 3.19 Measured waveforms of the input current of :(a) Config.3 and (b) proposed CFC at the same output power

In addition to the resonant frequencies f_{r1} and fr_2 caused by the resonant Circuits I and II, another ringing in the input current around 250 kHz was noticed due to the interaction between the boost inductance, stray capacitance of the boost inductor, and the clamp switch parasitic capacitance C_{pc}. Fig. 3.19a and b show the impact of this ringing on the input current of both Config.3 and the proposed converter. This ringing significantly restricts the sampling instant of the ADC converter, as shown in [10], and distorts the readings of the ADC converter.

To reduce the ringing problems caused by these resonant frequencies and thus improve the efficiency and the converter performance, different solutions have been developed in this work, as described next.

3.3.1.3 Remedies to Overcome the Effects of Parasitic Elements

Modification A

As indicated in the previous Section, a number of problems were observed with the existing FBCFC depicted in Fig. 3.8. The first step to further improve the performance of the proposed converter was to redesign the layout of an existing converter. This has been done by first isolating the electronic circuits such as MOSFETs, driver circuits, PWM scaling circuit (see Appendix B), signal condition unit SCU, and the DSP from the passive components, as indicated in Fig. 3.20. Then all the converter parts were positioned as close to each other as possible, and care was taken in laying out and fully screening the converter to avoid interference from the radiated RFI sources.

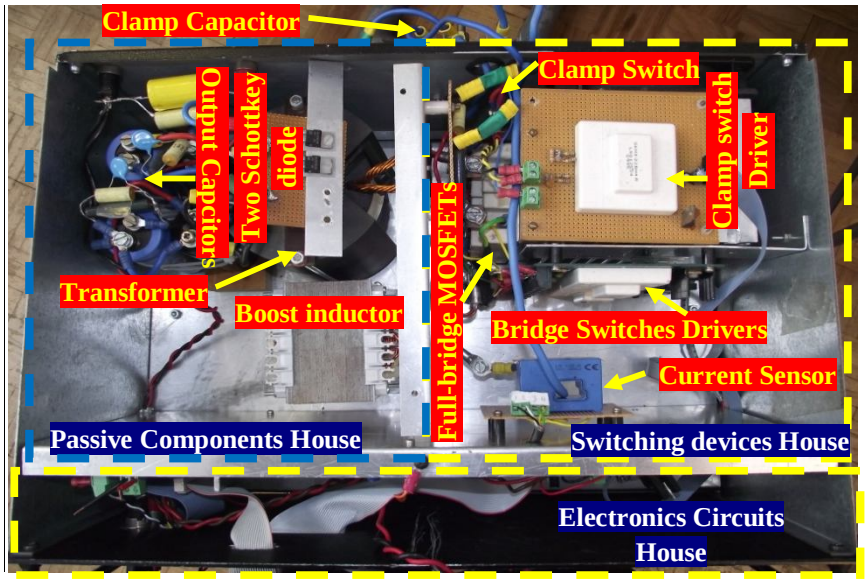


Fig. 3.20 Proposed converter with a new layout set-up

With this modification high frequency noise noticed on the PWM signals (Fig. 3.18a) and output voltage (Fig. 3.18b) caused by “Resonant Circuits II” has been considerably reduced (see Fig. 3.22a (ch1) and Fig. 3.23a).

Modification B

It is claimed in literature [55] that by interleaving the primary and secondary windings of isolation transformer the peak MMF values between the windings can be minimised, so the magneto-static energy which is not coupled to the secondary is reduced. Thus a lower leakage inductance can be achieved, which may obviate the need for an active clamp circuit in the CFC. The modelling and experimental results in Section 3.3.1.2, have shown that this is not necessarily true for all applications. It can be useful for low-power applications such as the 150W converter described in [55]. This is because of the following reasons:

1. It is hard to obtain a very low leakage inductance for the specifications of the present high-power FC converter system [103].
2. To ensure wide ZVS range for the switches the energy that is stored in the leakage inductance must be sufficient to fully charge and discharge the MOSFET parasitic capacitances especially at the light load. This is becomes a critical issue if the transformer has been designed with a very low leakage inductance value.
3. The leakage inductance reduction using the interleaving arrangement is accompanied by an increase in the winding-to-winding capacitance and the stray capacitance of the transformer [104]. This results in undesirable ringing effects and can produce in-circuit EMI noise and electrostatic coupling to other circuits, leading to reduce the converter performance and efficiency as a consequence.

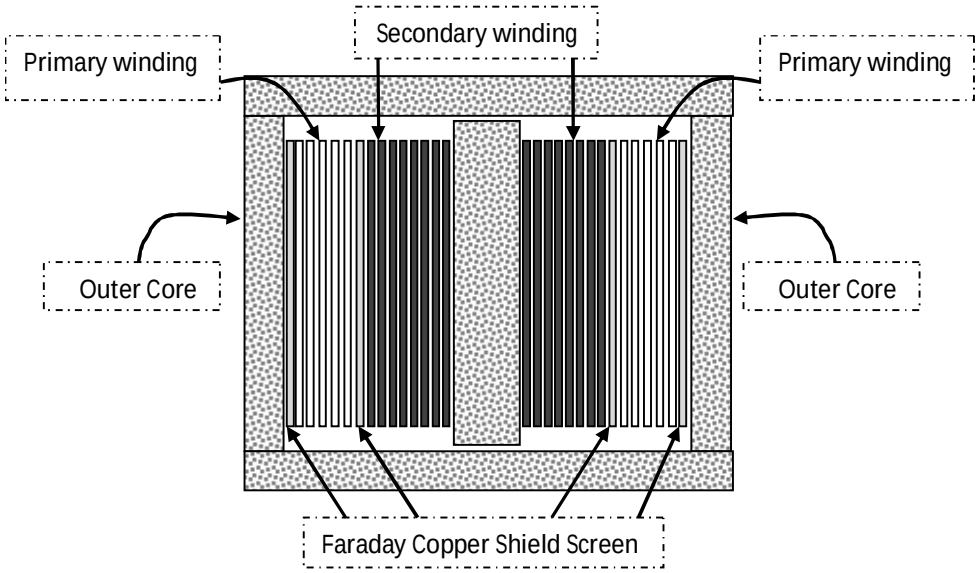


Fig. 3.21 Modified transformer-winding configuration using Faraday shield screen

For those reasons, the existing transformer was redesigned with an earthed Faraday shield screen, which was placed between the primary and secondary windings and between the outer core and the primary windings, as shown in Fig. 3.21. This arrangement keeps the leakage inductance as low as possible (only 2μH) without affecting the transformer winding-to-winding and stray capacitance values.

To transfer 1.2kW from the FC source of 26V, the transformer is designed with five primary turns and 37 turns on the secondary. The Faraday shield screen has also been applied to the boost inductor to reduce the ringing effect at the switching instant (see Fig. 3.19).

Modification C

As indicated in Chapter 2, the DC-DC converter is required to connect the low-voltage (26-42V), high-current (46A) FC power source to the high-voltage (650V) DC link. Hence, the current of the rectifier diodes at the DC link side is just a few amperes. This means that the dominant losses in the rectifier diodes are due to the switching losses.

The latter losses are related to the reverse-recovery charge (Q_{rev}) in the diode and the reversed-bias voltage across the diode. These losses can be minimised by either slowing down the slew rate of the diode current (with a reduction in the reverse-recovery charge as a consequence) or by minimising the ringing generated by the "Resonant Circuit II" (with a reduction in the reversed-bias voltage across the diode).

For that reason, a third modification has been developed by replacing the existing rectifier diodes with Schottky diodes (C2D05120A). These diodes have a very low reverse recovery current and a small parasitic capacitance (455 pF) which can help, with design approach B, to reduce the EMI noise, peak reverse voltage and switching loss as a consequence. These diodes can also operate at high frequency with low forward voltage drop resulting in a significant reduction in the conduction losses.

Modification D

Using switching devices with very low stray inductances and parasitic capacitance for the bridge and clamp circuits is one of the effective solutions to reduce the ringing produced by the "Resonant Circuit I" and improve the converter's efficiency. New power switching devices based on Gallium Nitride (GaN) technology can be considered instead of the existing SEMIKRON MOSFETs. Unfortunately, the cost of GaN devices is still very high and they are not readily available from suppliers.

A RC snubber circuit would be effective in reducing the ringing and therefore clamp the voltage spike across the clamp switch, by absorbing the circulating energy, thus reducing the switching losses. Unfortunately, dissipation of the circulating energy in the snubber will reduce the converter efficiency. However, the efficiency reduction is not excessive (for C=2.2nF the dissipated power in the snubber resistance R is about 0.88W) compared to the severe ringing generated by the "Resonant Circuit I" (see Fig.

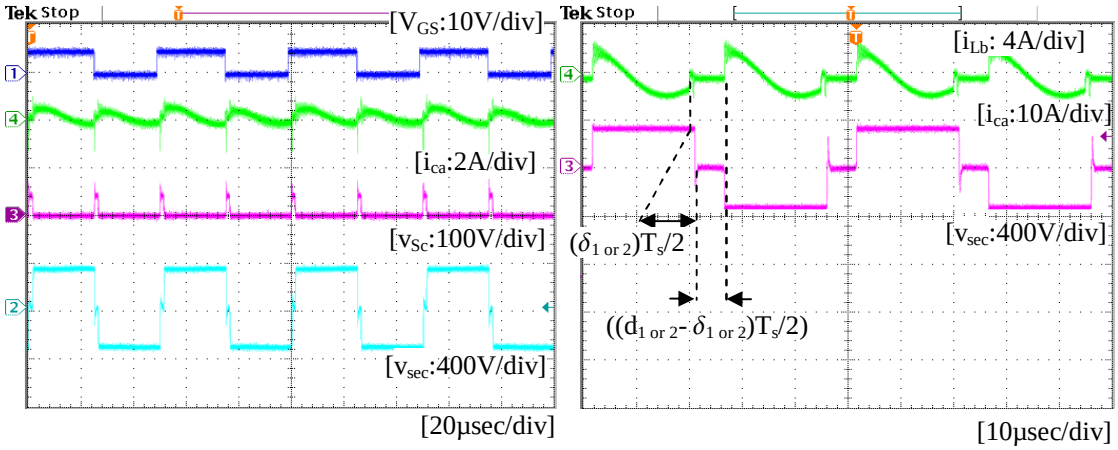
3.16) across and through the clamp circuit. Hence, the final arrangement for optimising the converter performance has been the addition of an RC snubber across clamp switch S_c.

3.3.1.4 Validation of the PSpice Model with the Developed Modifications

The objectives of this section are:

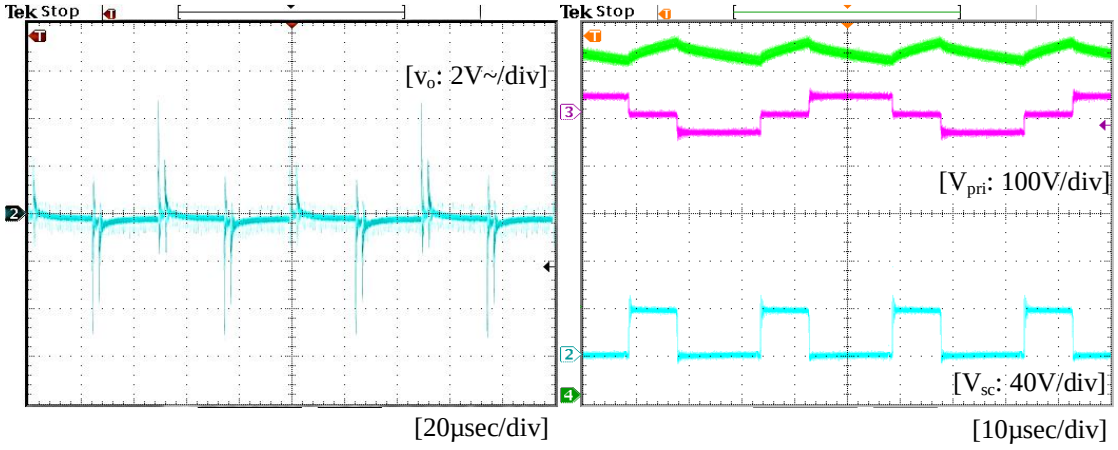
- Evaluate the converter performance with the modifications developed in Section 3.3.1.3.
- Show current and voltage waveforms of the converter with all the modifications implemented to prove that they have the desired effect.
- Compare the measured results with a limited number of waveforms obtained from a PSpice model that includes the modifications, in order to validate the PSpice model.

Fig. 3.22a and b show the measured waveforms of the current through the clamp circuit i_{ca} , the voltage across the secondary windings V_{sec} , the clamp switch voltage v_{ca} , and the gate signal V_{GS} at the output of the DSP at 4% and 30% of the full-load respectively. Due to the design modifications A, B, C and D, it can be seen that the current stress via the clamp circuit during the period $(\delta_{1or\,2})T_s/2$ and the ringing during the period $((d_{1\,or\,2}-\delta_{1\,or\,2})T_s/2)$ have been significantly reduced. Due to the lower transformer ringing the rectifier diodes are experiencing a reduced reversed-bias voltage, helping to decrease the reverse-recovery losses. In addition, the reduction in the transformer ringing improved the quality of the PWM gate signals at the output of the DSP and the driver circuit, as shown in Fig. 3.22a (ch1) and Fig. 3.24 (ch2) respectively.



(a) (b)

Fig. 3.22 Measured current and voltage waveforms of (a) From the top: DSP PWM gate signal V_{GS}, clamp current i_{ca}, clamp switch voltage V_{Sc} and secondary voltage v_{sec} at 4% of the rated power (b) From the top: clamp current i_{ca} and secondary voltage v_{sec} at 30% of the rated power



(a) (b)

Fig. 3.23 Measured current and voltage waveforms of (a) Output voltage ripple (b) From the top: the primary voltage v_{pri} , input current i_{Lb} , and the clamp switch voltage V_{sc}, at 70% of the rated power

Fig. 3.23a shows that the AC voltage ring on the DC link is reduce to 4V, compared with 6.4V for the converter without using the developed modifications (Fig. 3.18b). It can be observed from Fig. 3.23b, Fig. 3.24 (ch4) that the high frequency ringing through the input current is considerably reduced in comparison to the input current in Fig. 3.19b. Also the AC input voltage ring is only 0.4V, as shown in Fig. 3.24 (ch3).

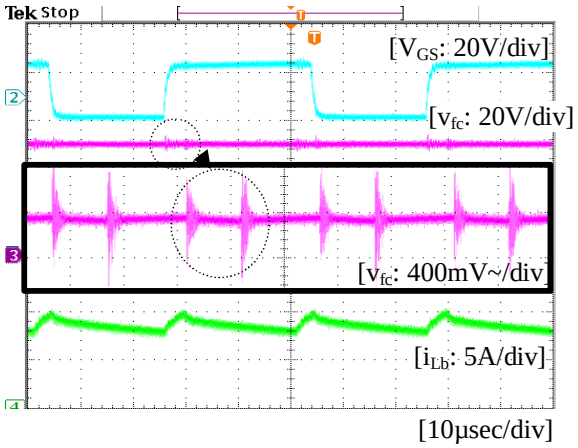
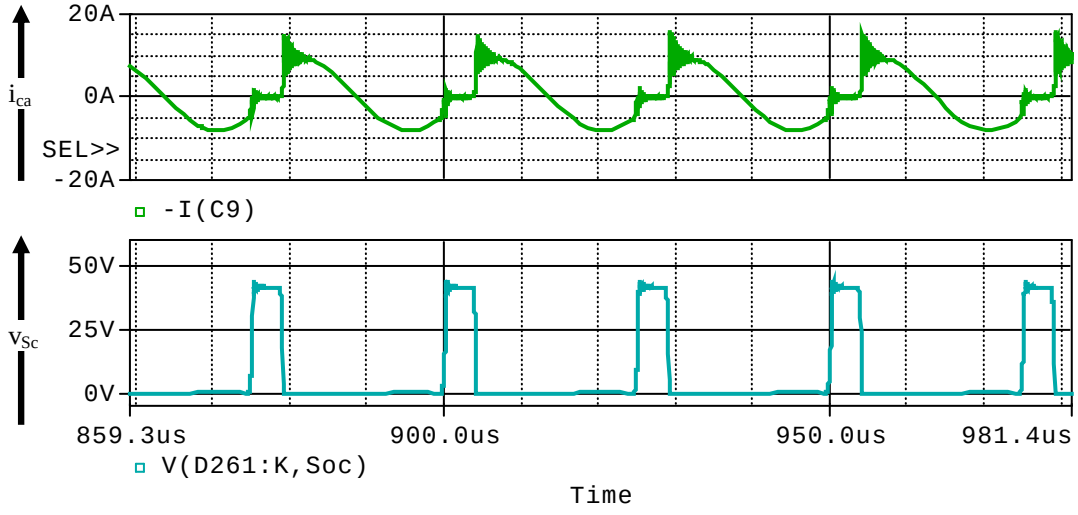


Fig. 3.24 From the top: measured waveforms of PWM gate signal at the output of MOSFET driver V_{GS}, input voltage and expanded view of (ch3) v_{fc}, and input current i_{Lb}

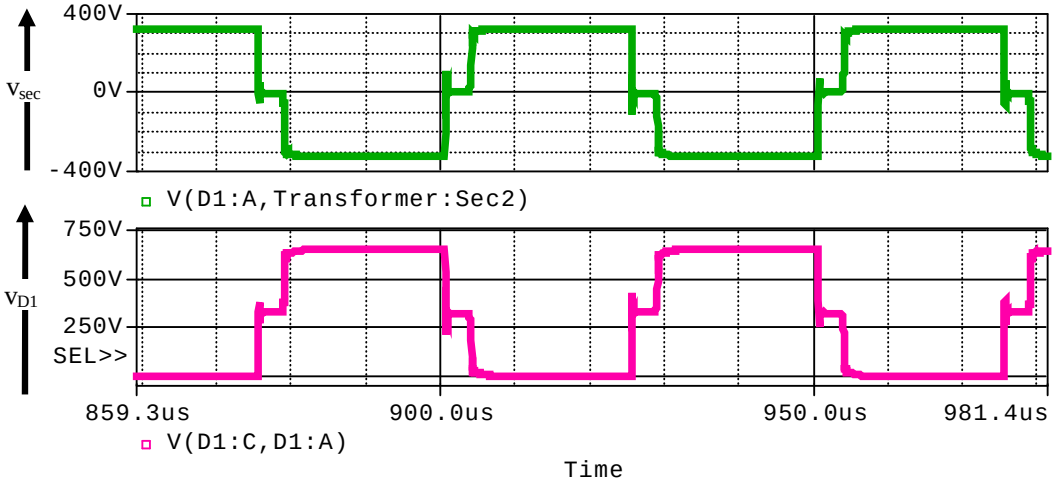
This reduction has been achieved by removing the flyback winding from the converter circuit (see Fig. 2.30, Fig. 3.8, and Section 3.3.1) and shielding the boost inductor through a Faraday screen.

Waveforms of the PSpice model are shown in Fig. 3.25. Compared with the measured results in Fig. 3.22–Fig. 3.24, it can be seen in Fig. 3.25 that with the new arrangements both the ringing effects of “Resonant Circuit I” and “Resonant Circuit II” are significantly reduced. Hence, the PSpice model confirms the practical results (and it can therefore be used with confidence for the investigation of an optimisation of the active-clamp circuit in the next section).

In summary, the waveforms presented in Fig. 3.22–Fig. 3.25 demonstrate that the developed modifications greatly improved the converter performance .



(a)



(b)

Fig. 3.25 Simulation waveforms show : a) From the top: clamp switch voltage and clamp current, b) From the top: voltages across the secondary winding and the rectifier diode

3.3.2 Optimisation of Active-Clamp Circuit

Whilst the active-clamp circuit is effective in suppressing the voltage overshoot across the bridge (Section 3.2.1), the active clamp can produce a peak current of up to twice the average input current because the energy absorbed in the clamp capacitor is recovered to the load via the main switching devices. Since the clamp switch operates at the twice the switching frequency, the switch turn-off losses can contribute significantly

to the total switching losses. Therefore, in [56] zero-current soft-switching at turn-off for the clamp switch has been proposed by selecting a smaller clamp capacitance value and using the resonance between C_a and L_σ. However, as will be shown this resonant scheme results in an increased current stress in the switches and the clamped voltage level is considerably higher than the voltage across the primary transformer windings requiring a higher voltage rating of the switching devices.

This section presents a novel approach for the selection of the clamp capacitor value that enhances the performance of the proposed converter. Modelling and theoretical analysis of the developed approach reveals that the voltage spikes across the clamp switch and bridge switches can be avoided, and the maximum device voltage is limited to a value slightly above the reflected output voltage on the transformer primary side. In addition, lower peak currents and circulating energy are realized, while achieving zero-voltage switching (ZVS) at turn-on for the full-bridge switches and near-zero current switching (near-ZCS) at turn-off for the clamp switch. The proposed method has been investigated in both Config.3 and the proposed CFC. The calculated and measured results of both configurations are compared and presented.

3.3.2.1 Analysis of the Proposed Method

During each period where a pair of diagonal switches is switched off, the proposed CFC in Fig. 3.1 can be presented by the equivalent circuit in Fig. 3.26. The same holds also for Config.3 , except that the reflected secondary voltage is then equal to V_o/n. During this interval the current through L_σ and the voltage across the clamp capacitor are described by:

$$i_{L\sigma}(t) = i_{Lb} - i_{Ca}(t) \tag{3.38}$$

and

$$v_{Ca}(t) = L_{\sigma}\frac{di_{L\sigma}(t)}{dt} + \frac{v_{C1}}{n} \tag{3.39}$$

where $i_{Lb} = \overline{I_{Lb}}$ (see assumptions (8) in Section 3.2.1) and $i_{Ca}(t) = C_a\frac{dv_{Ca}}{dt}$

This set of equations represents an undamped 2nd-order system with sinusoidal currents and voltages.

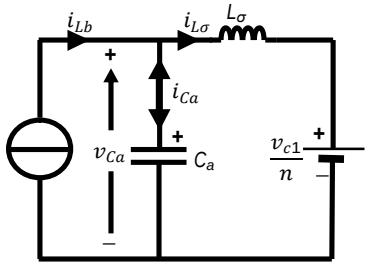


Fig. 3.26 Equivalent circuit diagram of the converter during the off-period of a diagonal bridge pair.

Since the initial condition is given by $i_{Ca}(0) = \overline{I_{Lb}}$ the solutions for i_{Ca} and v_{Ca} can be written as:

$$i_{Ca}(t) = \overline{I_{Lb}}\cos(\omega_o t) \tag{3.40}$$

and

$$v_{Ca}(t) = \sqrt{\frac{L_\sigma}{C_a}}\overline{I_{Lb}}\sin(\omega_o t) + \frac{V_{C1}}{n} \tag{3.41}$$

From (3.9) and (3.41), the maximum voltage across the clamp capacitor, the input bridge switches and the primary winding can be obtained as:

$$v_{Ca\_max}(t) = 2\pi f_0 L_\sigma\overline{I_{Lb}} + \frac{V_{C1}}{n} \tag{3.42}$$

It can be observed from (3.42) that if f_o is much higher than the switching frequency (f_s) (i.e. $f_o >> f_s$), the maximum clamp capacitor voltage (v_{Ca_max}) is considerably higher than the reflected output voltage on the transformer primary side. This occurs for small values of the clamp capacitance.

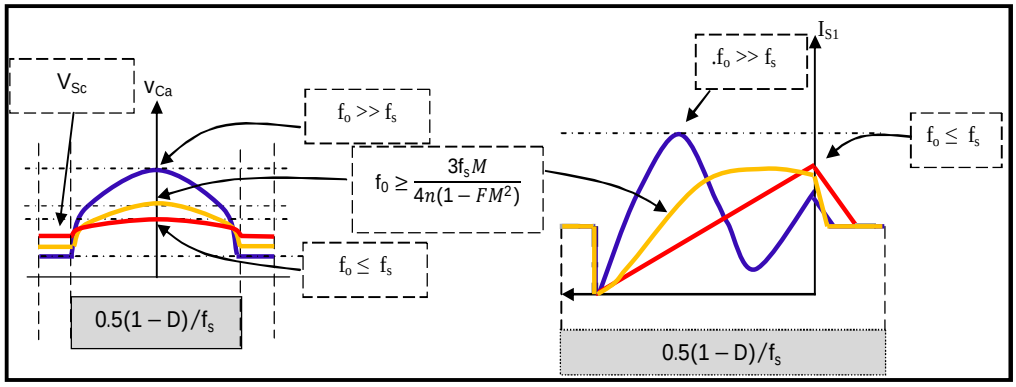


Fig. 3.27 Simulated waveforms of (a) clamp capacitor voltage and (b) switch current via S_1 for $f_o \leq f_s$, $f_o >> f_s$, and optimum C_a selection

Fig. 3.27a shows the waveforms of v_{Ca} for different values of f_o, obtained from simulations (see Section 3.3.2.2), which confirms that $f_o >> f_s$ results in an increased maximum clamp voltage. With the clamp switch closed the capacitor discharges through S_c due to the resonant. From (3.40) and (3.38) it follows that if $f_o > 2 f_s$ the peak current through the bridge switches can reach $2\overline{I_{Lb}}$. This is shown in Fig. 3.27b.

In order to obtain the lowest maximum clamp voltage, C_a could be selected at a high value so that $f_o \leq f$ [76]. While this results in a reduction in the peak clamp voltage as shown in Fig. 3.27a, this condition (i.e. $f_o \leq f_s$) leads to higher switching losses through the clamp switch at turn-off, as will be shown in the next section.

The presence of the active-clamp circuit thus leads to a circulating current at the input bridge side of the converter, which results in additional conduction losses. The amount of energy that is associated with the circulating current can be expressed as:

$$E_{Ca} = \frac{\overline{I_{Lb}^2} L_\sigma}{2} + \frac{\overline{I_{Lb}} V_o \sqrt{L_\sigma C_a}}{2n} \tag{3.43}$$

In Fig. 3.28 this circulating energy is plotted against the selected clamp capacitor value for both Config.3 and the proposed CFC configuration, where it can be seen that E_{Ca} greatly increases for the condition $f_o \leq f_s$ (large C_a), while at $f_o >> f_s$ (small C_a) a lower circulating energy is incurred. Equation (3.43) and Fig. 3.28 also show that the proposed converter leads to a considerable reduction in the circulating energy, with an associated reduction in conduction losses. In Fig. 3.29 the maximum value of V_{Ca} is plotted against the value of C_a, and it can be observed that for small values of the clamp capacitor (as e.g. proposed in [56]) V_{Ca} will be considerably increased, which is reflected in higher voltages across the full-bridge switches, the primary windings, and the high-voltage side devices.

It follows from the above analysis that the selection of the clamp capacitor will be a trade-off between the maximum clamp capacitor voltage (and hence the voltage rating of the full-bridge switches), the amount of circulating energy, and obtaining soft-switching operation of the clamp switch.

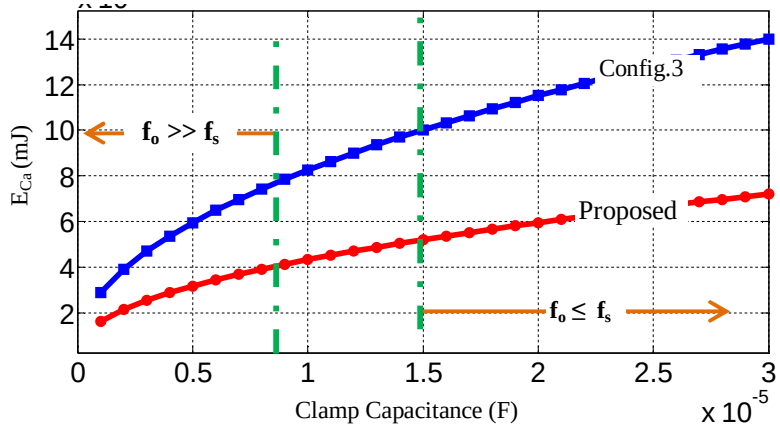


Fig. 3.28 Circulating energy caused by active-clamp circuit of the CFC in Config.3 and the proposed configuration ($\overline{I_{Lb}}$ =20A, and L_σ =2µH)

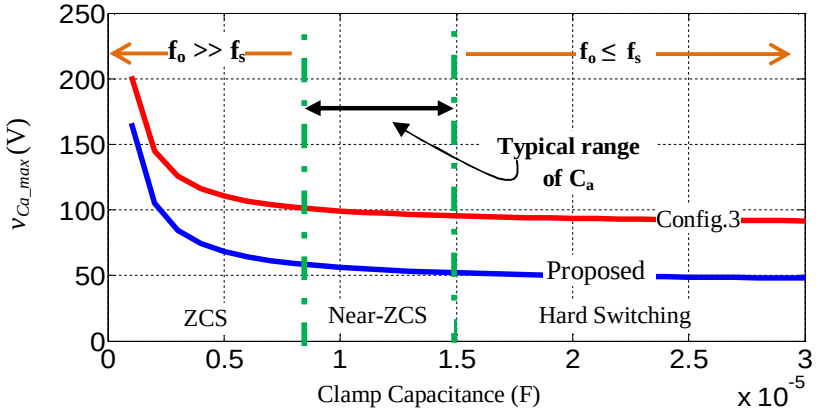


Fig. 3.29 Maximum clamp capacitor voltage for Config.3 and proposed ($\overline{I_{Lb}}$ =20A, and L_σ =2µH)

Since the maximum clamp voltage, switch peak current and stored active-clamp energy are determined by the relation between f_o and f_s, a new design approach for the active-clamp circuit is proposed here. This is based on taking a value for ratio of f_o and f_s, that lies between the values proposed in [56] and [76], corrected for the effective overlap duty cycle D_{eff}, i.e.:

$$f_0 \cong \frac{3f_s}{2(1-D_{eff})} \tag{3.44}$$

D_{eff} depends on the load conditions as well as the converter parameters as shown in (3.29). To incorporate these explicitly (3.44) can be expressed as:

$$f_0 \cong \frac{3f_sM}{4n(1-FM^2)} \tag{3.45}$$

where

$$F = \frac{2f_sL_\sigma}{R_o} \tag{3.46}$$

Therefore, based on the above condition C_a should be selected as:

$$C_a \cong \frac{4n^2(FM^2-1)^2}{9L_\sigma f_s^2 M^2 \pi^2} \tag{3.47}$$

According to Fig. 3.28 and Fig. 3.29 the typical range of the clamp capacitance that ensures optimum active-clamp circuit operation for the prevailing conditions is between 8 and 15µF. The optimum calculated clamp capacitance was selected as a10µF, 250V polyester film capacitor.

3.3.2.2 Simulation Results

For comparison, the three approaches to the design of the active-clamp circuit (i.e. $f_o >> f_s$, $f_o \leq f_s$, and the proposed approach) were simulated and analysed through PSpice/Simulink co-simulation using the SLPS interface (see Section 4.5.2 for further details about SLPS). The simulation model is shown in Fig. 3.30. The parameters that have been used in the simulation model are: V_{fc}=42V-26V, L_σ=2µH, n=7.4, f_s=20kHz, R_o= 603Ω, C_a=10µF, L_b=475µH C_1=C_2=500 µF.

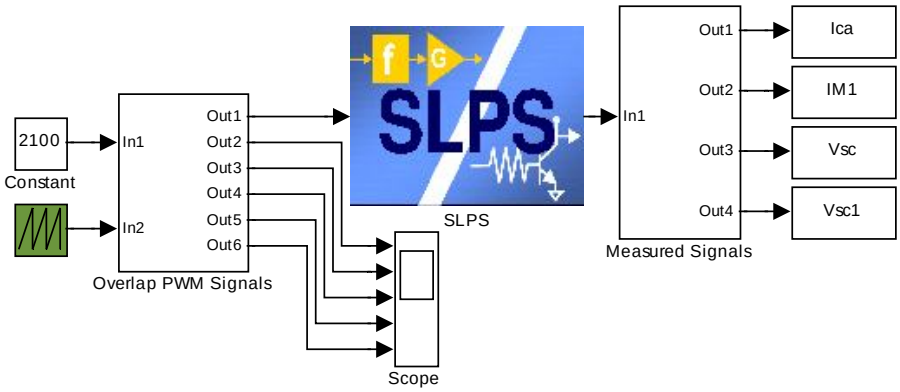


Fig. 3.30 Simulink block diagram with SLPS simulator used to evaluate the proposed active-clamp circuit design

In Fig. 3.31a it can be seen that for the condition $f_o \leq f_s$ a lower maximum voltage across the full-bridge switches is obtained. However, this condition not only leads to an increase in the clamp switch voltage v_{Sc} (see Fig. 3.31b), but also to higher turn-off losses, as can be seen from a close-up of the waveforms for the clamp switch voltage and current at turn-off of Sc, as shown in Fig. 3.32.

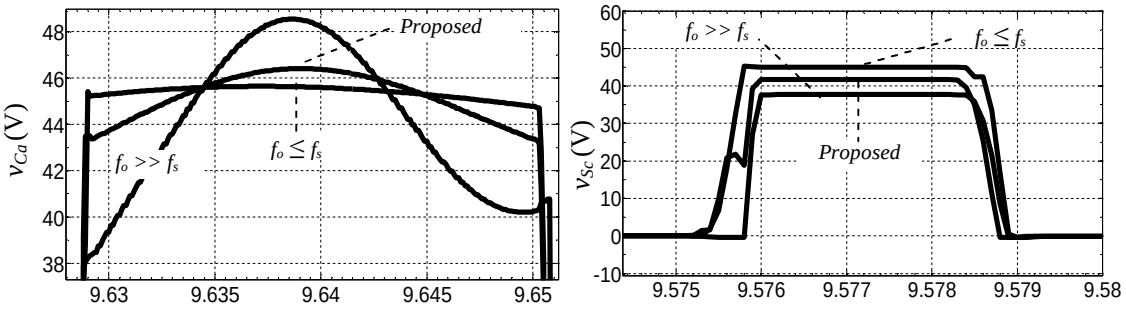


Fig. 3.31 Bridge switch voltage (a) and clamp switch voltage (b) for different choices of the resonant frequency.

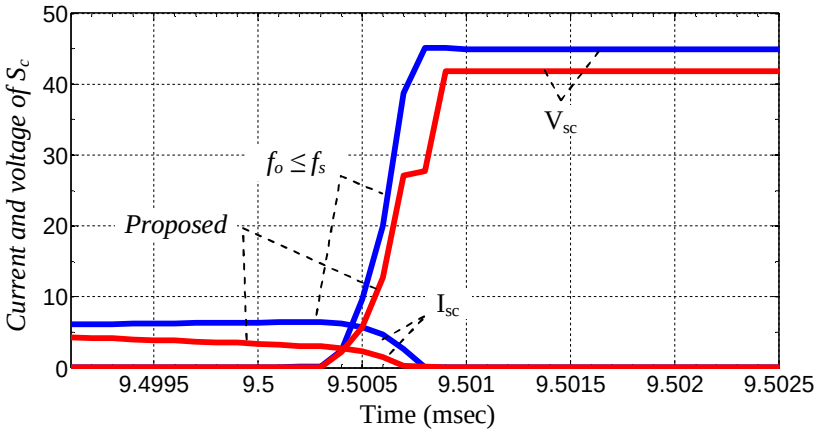


Fig. 3.32 Clamp voltage and current for different choices of f_o

This loss has a significant effect on the converter's efficiency since the clamp switch operates at twice the cycle frequency. Also, it is obvious from Fig. 3.33 that, if this condition is applied, a faster di/dt is imposed on the leakage inductance at turn-off.

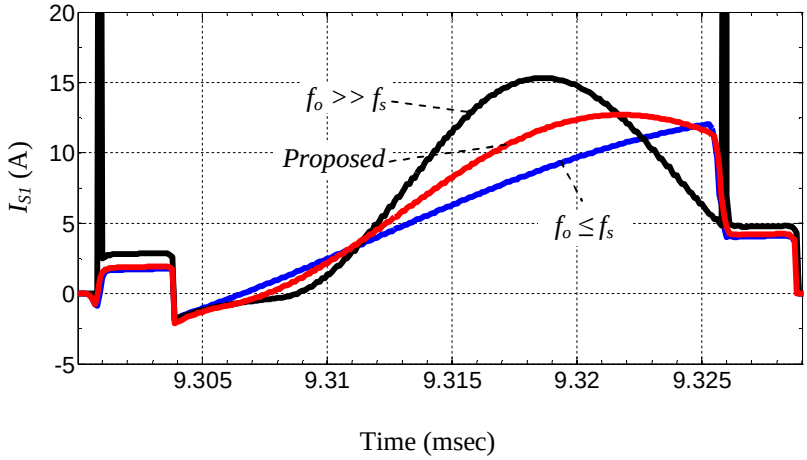


Fig. 3.33 Bridge switch (S_1) current waveforms for different f_o

To realize soft-switching for the clamp switch at turn-off, a lower clamp capacitance value (i.e. at the condition $f_o >> f_s$), was proposed in [56]. However, the analysis and simulation results show that this condition results in increased voltage stresses across the bridge switches, the clamp capacitor and the primary windings (see Fig. 3.31a). In addition, the converter components have to be rated at a higher peak current (see Fig. 3.33).

To solve the above drawbacks, the proposed active-clamp circuit design uses a new criterion to select the clamp capacitance value. This is based on the condition shown in (3.45). The simulation results demonstrate that the proposed method results in a value of v_{Ca_max} only slightly above the reflected output voltage on the transformer primary side, and near- ZCS at turn-off of the clamp switch. Also, as can be seen in Fig. 3.34 this approach slows down the rising of the diode current, resulting in turn-on the rectifier diode with zero-current.

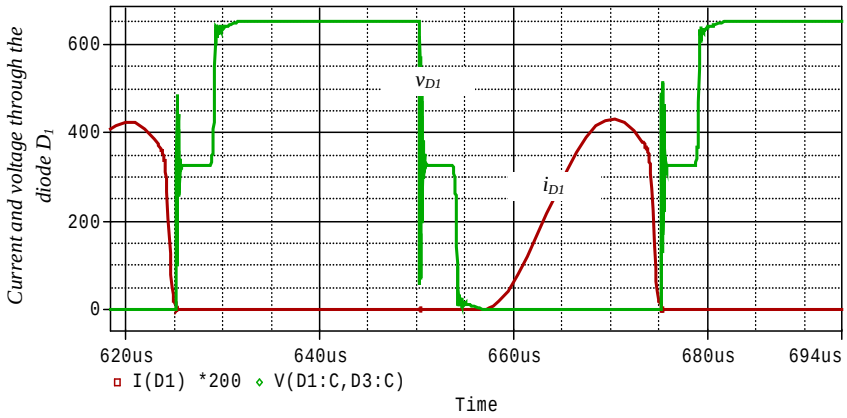


Fig. 3.34 Current and voltage waveforms of the rectifier diode D1

Fig. 3.35 compares the achievable efficiency for the three approaches based on the simulation results. It can be seen that, overall, the converter with the proposed design method has a better efficiency than the other two approaches, as its performance is maintained over the entire power range.

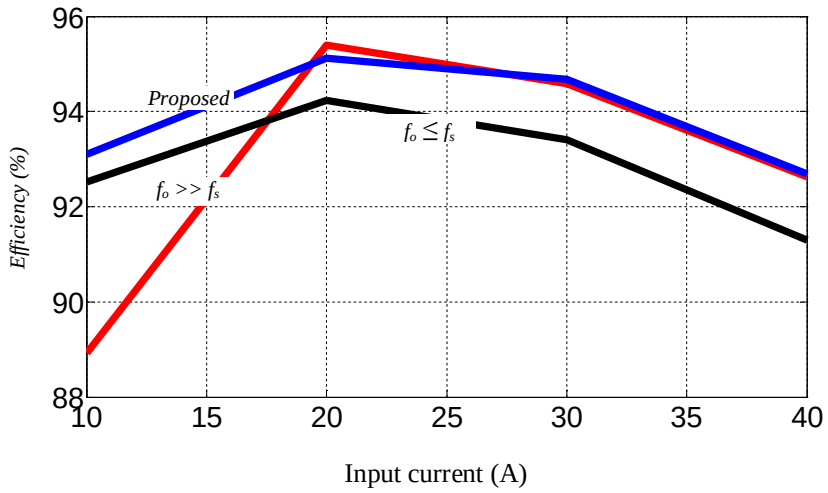
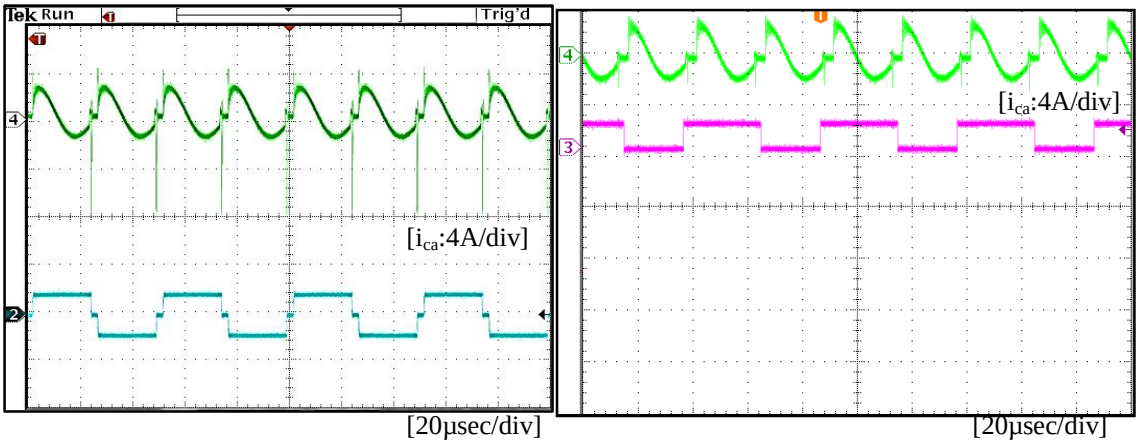


Fig. 3.35 Simulated efficiency comparison of the proposed CFC for different conditions, $f_o \leq f_s$, $f_o >> f_s$, and optimum C_a selection

The improvement over the approach with $f_o \leq f_s$ is due to the reduced switching losses, while the improvement over the approach with $f_o >> f_s$ at outputs less than the half of the rated power is the result of lower conduction losses.

3.3.2.3 Experimental Results

To verify theoretical and simulation results, the optimised active-clamp circuit has been implemented using the experimental set-up shown in Fig. 3.14.



(a) (b)

Fig. 3.36 Measured clamp current waveforms for a) $f_o >> f_s$ and b) the proposed approach

Waveforms of the clamp capacitance current for the conditions $f_o >> f_s$ and the proposed approach at 40% of full load are shown in Fig. 3.36a and b respectively. It can be seen (Fig. 3.36b) that the clamp capacitor current has a lower peak current using the proposed approach. The current waveform in Fig. 3.36a exhibits a very large peak current at the start of the bridge overlap period due to the discharge of parasitic capacitances of the MOSFETs. This phenomenon doesn't occur using the proposed approach.

3.3.3 Selection of the Dead time

It was observed through simulation and practical tests that if the dead time T_{dead1} was designed to be equal to the quarter of the resonant period between C_{p1}, C_{pc} and L_{σ}, as proposed in [57], a high voltage spike occurs across the clamp switch S_c while it is conducting. This can be observed in Fig. 3.37(bottom trace) and Fig. 3.38(top trace) respectively.

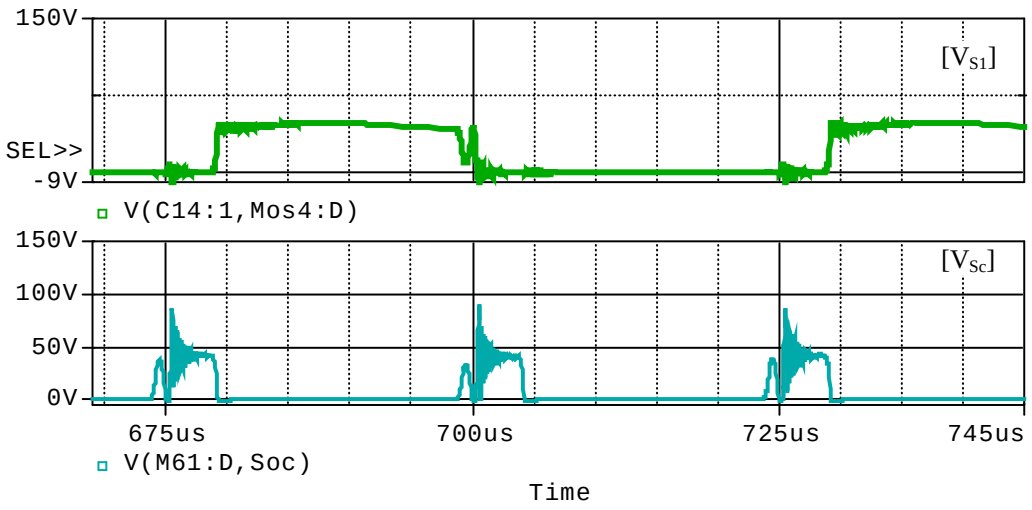


Fig. 3.37 Simulation waveforms of the voltage across the bridge switch S_1 and the clamp switch S_c

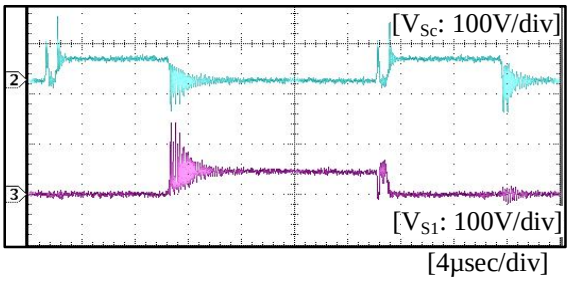


Fig. 3.38 Measured waveforms of the voltage across the clamp switch S_c and the bridge switch S_1

The reason of this is that the duration T_{dead1} is insufficient to permit full charging and discharging of C_p and C_{pc} by the energy stored in the leakage inductance L_σ.

Therefore, it is found that an optimum selection of this duration T_{dead1} is achieved when the condition in (3.31) is applied. Notice the elimination of this voltage spike in Fig. 3.23b (ch2). This dead time duration has been adjusted by activating the dead zone option in the DSP as described in Appendix H.

3.4 Comparative Results

To evaluate the features of the proposed converter, a comparison has been carried out between the converter and other competing FBCFC, such as Config.1 (see Fig. 2.23b), Config.2 (see Fig. 2.26), and Config.3 (see Fig. 2.29c). The comparison with Config.3 is not directly comparable, but was based on pre-existing laboratory prototype at the same power rating in according to the parameters in Table 3.3.

TABLE 3.3
ACTIVE-CLAMPED CFC PARAMETERS

Parameters	Config.1	Config.2	Config.3	Proposed
Transformer turns ratio (n)	8.85	7.4	8.85	7.4
Output capacitor voltage	650V	325V	650V	325V
Leakage inductance (L_σ)	4µH	2µH	4µH	2µH
Switching frequency (f_s)	20kHz	20kHz	20kHz	20kHz
Fuel cell voltage (V_{fc})	26-43V	26-43V	26-43V	26-43V
Load Resistance (R_o)	352Ω	352Ω	352Ω	352Ω
Internal fuel cell resistance (R_{fc})	0.35Ω	0.35Ω	0.35Ω	0.35Ω
Clamp capacitance (Ca)	N/L	N/L	10 µF	10 µF
Output capacitor	1100µF	500µF (two)	1100µF	500µF (two)
Boost inductance (L_b)	475 µH	475 µH	475 µH	475 µH
Rectifier Diodes	Fast recovery	Fast recovery	Fast recovery	SiC Schottky

3.4.1 Evaluation of the Proposed FBCFC Features

The simulation model in Fig. 3.30 and the hardware set-up (with the optimisation and modification approaches of Section 3.3) have been used to compare the performance of the converter with other FBCFC. It can be seen in Fig. 3.39, that with the proposed CFC the voltages for the clamp capacitor C_a, the clamp switch S_c and the bridge switches S_1~S_4, for different turns ratio as indicated in Table 3.3, are 1.6 times less (44V) than that of the Config.3 (74V).

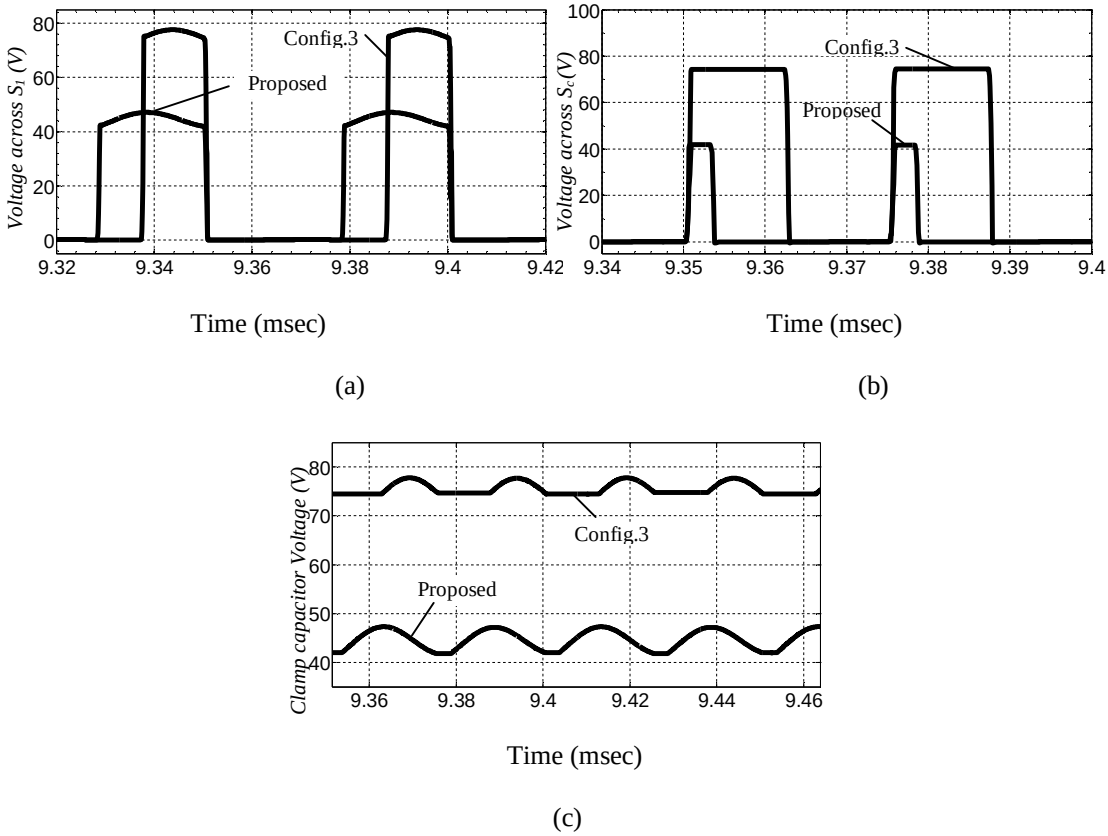


Fig. 3.39 Simulated waveforms of a) bridge switch voltage (S_1) b) clamp switch voltage and c) clamp capacitor voltage for the Config.3 and proposed configurations

This can also be observed in the clamp capacitor voltage v_{Ca} of Fig. 3.41(a and b). However, the voltage rating of the switching devices of Config.1 and Config.2 could be reached up to the maximum rating of the switch as in Fig. 3.40a and b. Hence, the proposed converter has the ability to work with device ratings of less than 80V and therefore the parasitic elements can be reduced significantly. In addition, the turn-off

loss of bridge switches of the converter is much less than in Config.3. This is because the voltage across the bridge switches at the turn-off is only about 44V compared to 74V for the Config.3. Thus, a highest operating efficiency can be achieved.

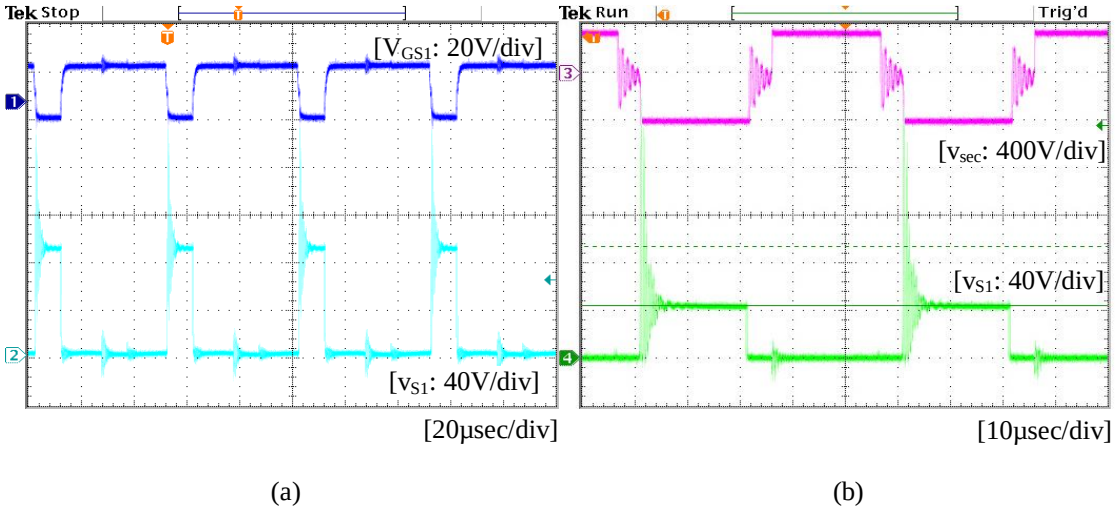


Fig. 3.40 Measured waveforms of (a) Config.3: secondary and primary voltages, (b) Config.2: Secondary voltage and voltage across the bridge witch S_1

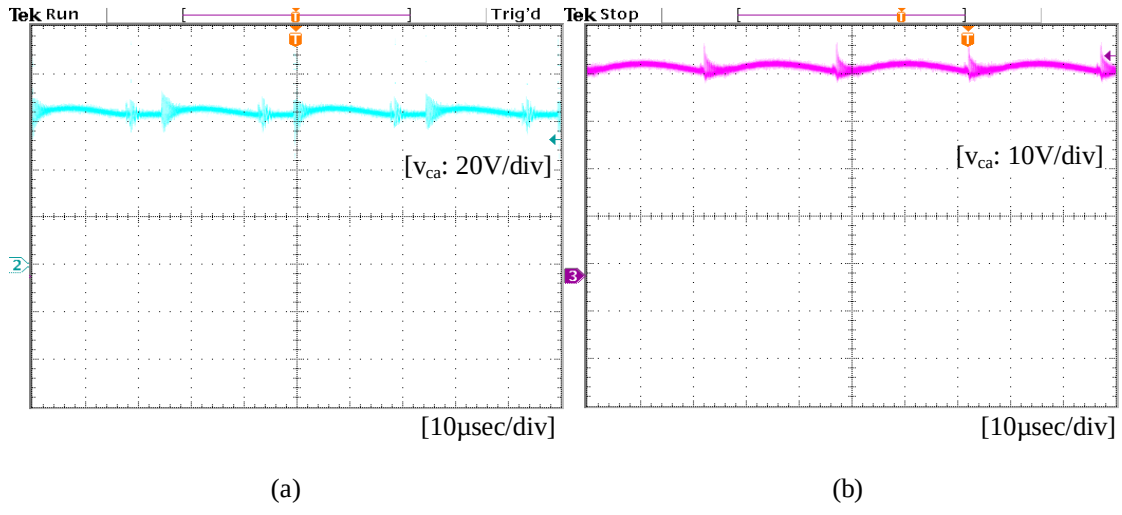


Fig. 3.41 Measured waveforms of the clamp capacitor voltage of (a) Config.3 and (b) proposed configurations

Fig. 3.39a and Fig. 3.19 also shows that to deliver a same power to the load, Config.3 requires a larger duty cycle than the proposed CFC. This means that the bridge switching devices conducts for a longer period than in the proposed CFC. Thus, higher

conduction losses will be incurred. In addition, for the same power during the overlap period the bridge switches have a shorter commutation period than in Config.3 as shown in Fig. 3.42b. The reduction in this period decreases the conduction loss of the bridge switches thus increasing the operating efficiency as a consequence (see Fig. 3.44).

Fig. 3.42a and b show the current through the boost inductor i_{Lb} and the bridge switch S_1 for both Config.3 and the proposed CFC. It can be seen that for the same average input current the proposed CFC exhibits a lower input current ripple, which has a positive effect on the FC lifetime. This was observed as well in Fig. 3.19.

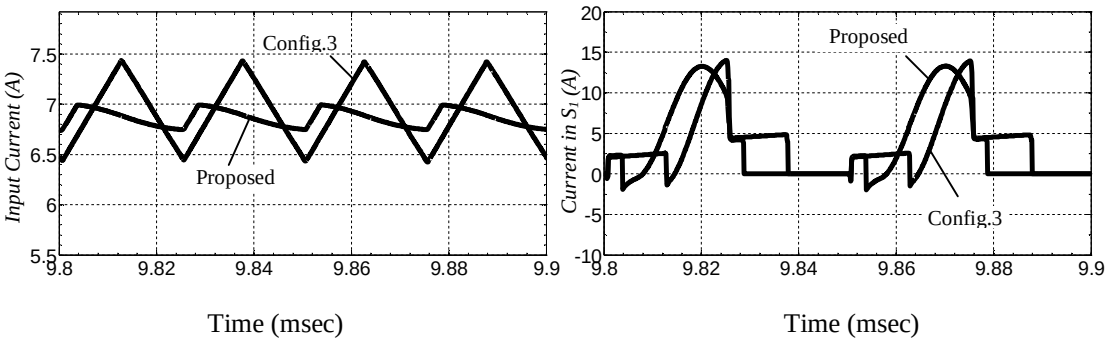


Fig. 3.42 Measured current waveforms through (a) input inductor i_{Lb} and (b) bridge switch S_1 for Config.3 and the proposed configuration

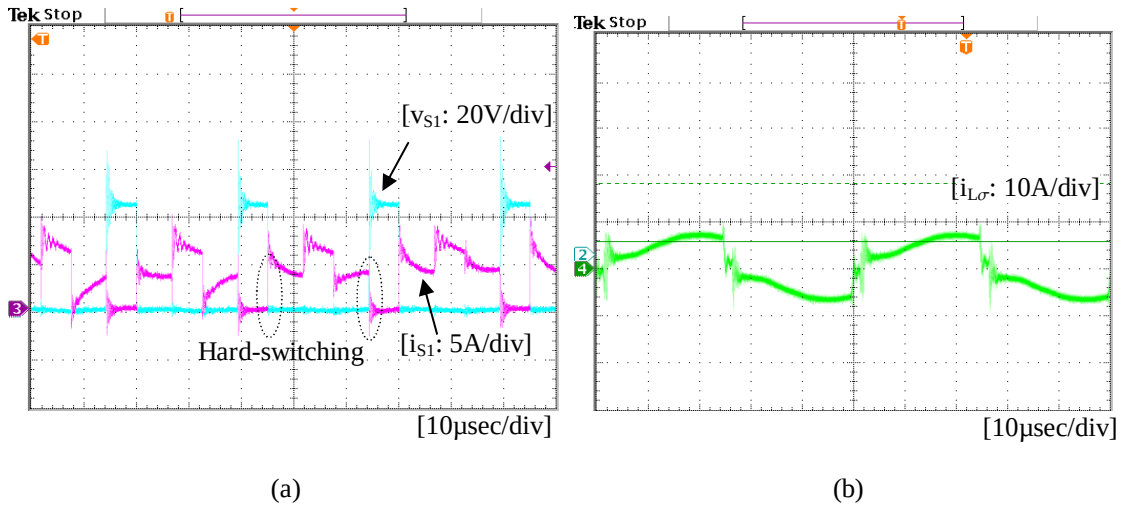


Fig. 3.43 Measured waveforms of the current through (a) the bridge switch S_1 of the Config.2 and (b) the primary of the proposed configurations at 200W

The corresponding waveforms for the current through the bridge switch S_1 and the transformer primary are shown in Fig. 3.43a &b. Due to the fast current switching (di/dt), Config.2 exhibits a high voltage overshoot and hard-switching operation for the bridge switches.

3.4.2 Efficiency Comparison

To evaluate the actual efficiency of the proposed converter, a comparison has been carried out between the performance of different CFC topologies, using both PSpice-based simulation and practical tests.

The total converter losses P_{loss} are calculated as the sum of the switching losses and conduction losses for the clamp switch, bridge switches and the rectifier diodes as shown below

$$P_{Total} = P_{cond\_T} + P_{Swit_T} + P_{diode\_loss} \tag{3.48}$$

where the switching losses P_{swit_T}, conduction losses P_{cond_T}, and diode loss P_{diode_loss} are defined as

$$P_{Swit\_T} = P_{Mos\_On} + P_{Mos\_Off} = 4E_{sw}f_s + E_{sw\_c}(2f_s) \tag{3.49}$$

$$P_{cond\_T} = P_{Mos\_cond} + P_{anti-diode_{cond}} = 4I^2_{RMS\_S1,S4}R_{ON} + I^2_{RMS\_Sc}R_{ON} \tag{3.50}$$

where E_{sw} and E_{sw_c} is the energy dissipated through the main and clamp switching devices during switching instants, $I_{RMS\_S1,4}$ and I_{RMS_Sc} are the RMS currents of the bridge and clamp switches respectively, R_{ON} is the MOSFETs on-resistance, are obtained from the datasheet as shown in Table 3.2, and

$$P_{diode_{loss}} = Q_{rev} V_{RB} f_s + I_F V_F \tag{3.51}$$

where Q_{rev} is reverse-recovery charge, and V_{RB} is reversed-bias voltage of the diode.

The efficiency $\eta = P_o / P_{in}$ of the compared topologies is then calculated with output power equal to (P_{in}-P_{loss}). The total losses P_{loss} for Config.2, Config.3, and the proposed configuration are presented in Fig. 3.44.

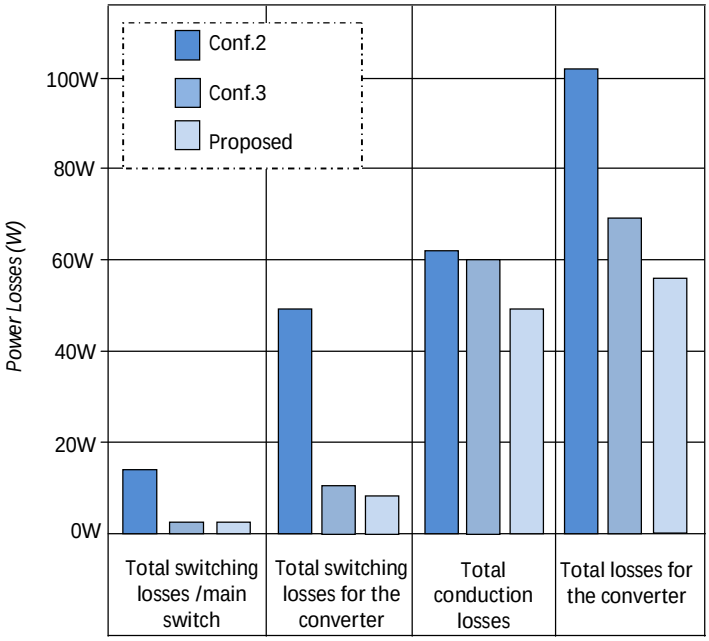


Fig. 3.44 Calculated power losses of three CFC configurations for operation at 1kW

The converter efficiencies for Config.1, Config.2, Config.3, and the proposed configuration with and without the developed modifications obtained from the simulation and practical tests for different operating points are shown in Fig. 3.45. It can be seen that with the modifications developed in Section 3.3.1.3 the efficiency of the proposed converter has increased by 2% at 60% load. At light load, it can be observed that the efficiency of Config.3 and proposed configuration are close together. For high

load, the new converter is more efficient (around 1%)[16] than Config.3. This is because Config.3 has higher conduction losses since the bridge switches must (for the same power) remain on for a considerable longer period than that of the new converter during one cycle (see Fig. 3.39a and Fig. 3.42b). In addition, Config.3 has higher copper losses in the transformer windings due to the higher turns ratio.

It can be seen that the efficiency for Configs. 1 and 2 is measured only up to 880W. This is because the switching devices reached to their maximum rating voltage at this power due to the high overshoot voltage (up to 200V, see Fig. 3.40a and b). As shown in Fig. 3.45, the efficiency comparison shows a good agreement between the simulation and measured results.

By combining the following techniques: 1) the voltage-doubler, 2) the clamp circuit 3), the developed modifications, and 4) the proposed optimization of the clamp circuit, the simulation and experimental results showed that the new converter operates with the lowest losses. These techniques significantly helped in reducing the voltage rating of the converter components and the energy that is dissipated in it, and result in an increased converter efficiency (up to 96%).

[16] The new converter is designed and compared with the Config.3 using the same full-bridge with the same clamp and bridge switches. However, if existing switches are replaced with switches that have a lower voltage rating, a further improvement in efficiency can be achieved for the proposed converter. This is because Config.3 experienced a higher drain to source voltage across the switches than the proposed CFC, resulting in higher switching and conduction losses.

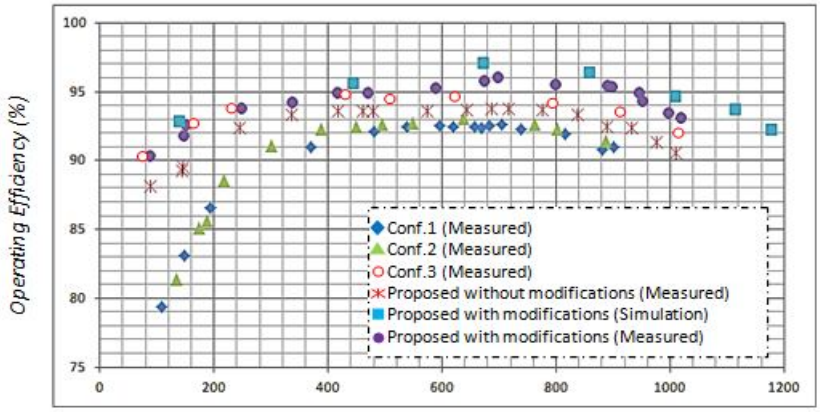


Fig. 3.45 Simulated and measured efficiencies for different FBCFC configurations

3.5 Conclusions

A new FBCFC configuration has been analysed and compared with other potential topologies for use as a DC-DC converter for connecting a FC power source to the DC bus of a DC microgrid. Simulation and practical tests have shown that the proposed converter is 2% more efficient than the conventional CFCs such as Config.1, 2 and 3 over the entire load range. Also the converter reduced the energy circulation in the clamp capacitor to half that of the Config.3 (less than 5mJ at the 60% load) and has the lowest voltage stresses across the MOSFET switches (less than 50V compared to 74V for Config.3 and 200V for Config.1 and 2 at the 100% load). Also, the converter provides ZVS for the bridge switches and clamp switch in addition to the ZCS at the turn-on and turn-off of the rectifier diodes which significantly eliminated the revere-recover losses of the voltage-doubler rectifier diodes.

Based on the PSpice simulation and hardware implementation of the converter, it has been observed that during the overlap period the parasitic elements create undesirable oscillations in the voltage and current through the converter which can be categorised as follows:

- Voltage ringing across the clamp switch and oscillating in the current via the clamp circuit are occurred whenever the clamp current reached zero
- Voltage ringing across the bridge whenever the voltage reached zero
- A lightly damped oscillating across the diodes rectifier and secondary winding
- EMI noise interference with the DSP and other electronic circuits, and
- High ringing through the input current at the switching instants.

It has been found that these oscillations created unnecessary circulating energy which results in reduced the converter efficiency, particularly at the light load (see Fig. 3.45). Methods to mitigate these effects have been described, together with their impact on converter performance and EMI suppression.

In addition, results from simulations and measurements on a prototype converter have shown that designing the active-clamp circuit with a high resonant frequency (i.e. a small clamp capacitance value) can realize ZCS at turn-off of the clamp switch but leads to a higher voltage rating of the converter devices, higher peak currents, and a high current spike through the switches. In contrast, designing the active-clamp circuit with a low resonant frequency (i.e. a large clamp capacitance value) can reduce the voltage rating of the full-bridge switches but at the cost of higher switching loss in the clamp switch. It has also been shown that an appropriate choice of the resonant frequency between the transformer leakage inductance and the clamp capacitance in relation to the switching frequency can overcome all the above drawbacks. Therefore, an optimised active-clamp circuit design is proposed to further optimise the operation performance.

As predicted by the PSpice/SLPS analysis, by using the developed modifications and the clamp circuit optimisation, considerable efficiency enchantments were

experimentally observed (up to 2% at the 60% load) over the entire range of converter operation while keeping the simplicity of the configuration and superiority of the performance of the converter.

Chapter Four

Dynamic Modelling and Digital Control of a Fuel Cell Converter System

4.1 Introduction

In order for the proposed FC converter, described in the previous Chapter, to operate at the desired DC link voltage despite changes in system load and variations in the FC voltage, a closed-loop controller is required. Since the CFC is a non-minimum phase system, a two-loop controller is preferable to separate the RHPZ from the converter transfer functions, thus increasing the controller bandwidth, and protecting the FC system from high inrush current and ripple. To study the dynamic behaviour of the converter and design the required controller, a dynamic model for the converter is needed.

In the present chapter, an exact dynamic model for the proposed converter including the active-clamp circuit, the FC power source model, and the parasitic elements is developed. Using the dynamic model, the converter dynamic performance is evaluated and compared to other competing CFC configurations. A suitable digital average current-mode control for the converter has been designed, verified and implemented. The control system has been designed systematically for the converter derived from the developed dynamic model, while it is verified using a new co–simulation approach and implemented on the real hardware processor using the Model-Based Design (MBD) method.

4.2 Development of the Mathematical Dynamic Model

To facilitate the dynamic model derivation for the proposed CFC, the same assumptions as those introduced in Section 3.2.1 are used here. In addition to those assumptions, the state variables of the converter system must be determined. As defined in Fig. 3.1, the boost inductor/input current i_{Lb}, the primary current $i_{L\sigma}$, the clamp capacitor voltage v_{Ca}, and the voltage-doubler capacitor voltages v_{C1} and v_{C2} are chosen as state variables. Those variables can be written as a state vector $\vec{x}(t)$:

$$\vec{x}(t) = [i_{Lb} \quad i_{L\sigma} \quad v_{Ca} \quad v_{C1} \quad v_{C2}]^T \tag{4.1}$$

4.2.1 Derivation of State–Space Equations

In this section, the state-space equations for each operating mode indicated in Fig. 4.1 are derived. These equations are required in order to synthesis the small-signal state-space model (see Section 4.2.2), to derive the small-signal AC equivalent circuit (see Section 4.2.3), and to design an appropriate controller for the converter (see Section 4.4).

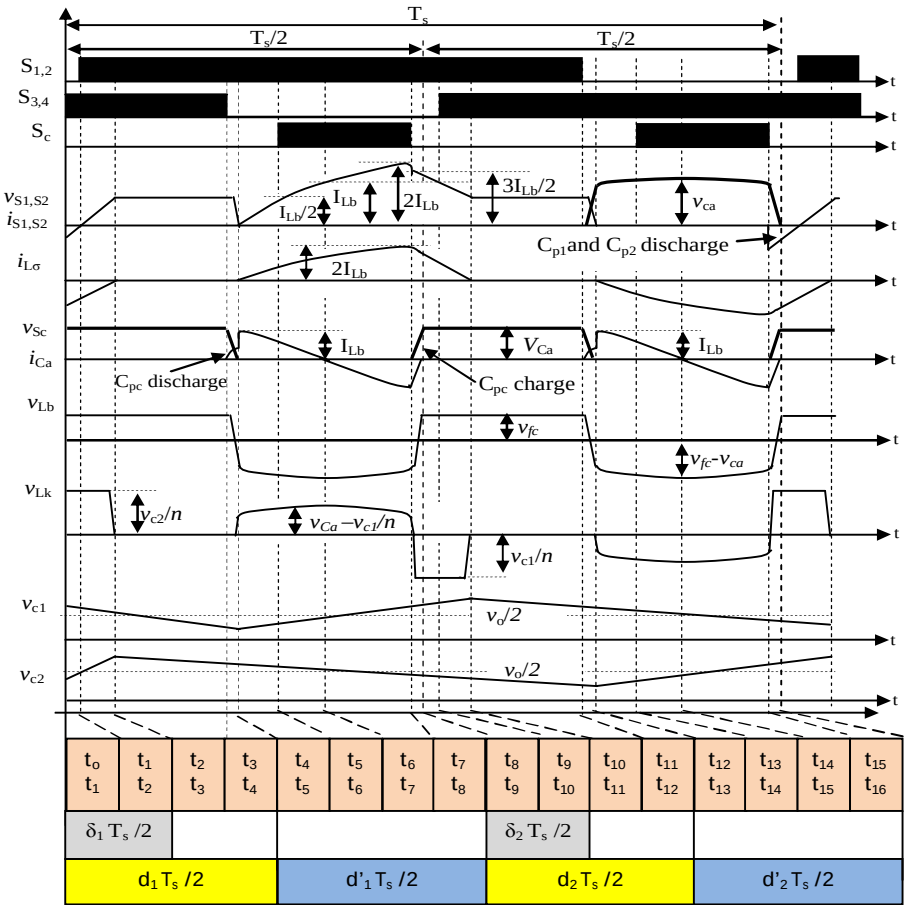


Fig. 4.1 Gate signals, voltage, and current waveforms of the converter

As can be seen in Fig. 4.1, the operation of the converter can be divided into 16 operating modes for one switching cycle (T_s) but because of the similarity of two half–cycles, only the first 8 modes are described here. The state-space equations for the first 8 operating modes are derived as follows [105]:

Modes $\in \{(t_0 < t < t_1)$ and $(t_1 < t < t_2)\}$: In these two modes the switches S_1 and S_2 are turned-on with ZVS and the energy stored in the leakage inductance is discharged and transferred to the secondary side for the period indicated as $(0.5\delta_1 T_s)$. From the equivalent circuit of modes T_1 and T_2 in Fig. 3.3 and using Fig. 4.1, the dynamic state-space equation is obtained as follows:

$$\begin{bmatrix} \frac{di_{Lb}(t)}{dt} \\ \frac{di_{L\sigma}(t)}{dt} \\ \frac{dv_{ca}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{nL_\sigma} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_1R_o} & -\frac{1}{C_1R_o} \\ 0 & \frac{1}{nC_2} & 0 & -\frac{1}{C_2R_o} & -\frac{1}{C_2R_o} \end{bmatrix} \begin{bmatrix} i_{Lb}(t) \\ i_{L\sigma}(t) \\ v_{ca}(t) \\ v_{c1}(t) \\ v_{c2}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_b} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_{fc}(t)] \quad (4.2)$$

According to the FC equivalent circuit model in Fig. 2.4, the FC terminal voltage ($v_{fc}(t)$) can be found as:

$$v_{fc}(t) = v_{fc\_o}(t) - i_{Lb}(t)R_{fc} \quad (4.3)$$

where $v_{fc\_o}(t)$ is the open-circuit voltage of the FC generator and $i_{Lb}(t) = i_{fc}(t)$.

Mode $\in \{(t_2 < t < t_3)\}$: In this mode the stored energy in the leakage inductance totally expended and the FC current will circulate through the H–bridge switches. The dynamics of this mode describe the following state-space equation:

$$\begin{bmatrix} \frac{di_{Lb}(t)}{dt} \\ \frac{di_{L\sigma}(t)}{dt} \\ \frac{dv_{ca}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_1R_o} & -\frac{1}{C_1R_o} \\ 0 & 0 & 0 & -\frac{1}{C_2R_o} & -\frac{1}{C_2R_o} \end{bmatrix} \begin{bmatrix} i_{Lb}(t) \\ i_{L\sigma}(t) \\ v_{ca}(t) \\ v_{c1}(t) \\ v_{c2}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_b} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_{fc}(t)] \quad (4.4)$$

Mode $\in \{(t_3 < t < t_4)\}$: This mode represents the charge/discharge interval of parasitic capacitances of the switches. During this mode these parasitic capacitances resonate with the leakage inductance to achieve soft-switching. Hence, neglect of this interval simply means that the converter is operating under hard–switching, which is incorrect as indicated in Section 3.2.3. Therefore, to accurately predict the dynamic behaviour of the converter, the developed dynamic model here takes into account this interval.

The state-space equation for this mode is given as:

$$\begin{bmatrix} \frac{di_{Lb}(t)}{dt} \\ \frac{di_{L\sigma}(t)}{dt} \\ \frac{dv_{ca}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_1 R_o} & -\frac{1}{C_1 R_o} \\ 0 & 0 & 0 & -\frac{1}{C_2 R_o} & -\frac{1}{C_2 R_o} \end{bmatrix} \begin{bmatrix} i_{Lb}(t) \\ i_{L\sigma}(t) \\ v_{ca}(t) \\ v_{c1}(t) \\ v_{c2}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_b} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_{fc}(t)] \quad (4.5)$$

Modes $\in \{(t_4 < t < t_5), (t_5 < t < t_6)$, and $(t_6 < t < t_7)\}$, these modes representing the operation period of an active clamp circuit. During this period the state-space equation is obtained as:

$$\begin{bmatrix} \frac{di_{Lb}(t)}{dt} \\ \frac{di_{L\sigma}(t)}{dt} \\ \frac{dv_{ca}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_b} & 0 & 0 \\ 0 & 0 & \frac{1}{L_\sigma} & -\frac{1}{nL_\sigma} & 0 \\ \frac{1}{C_a} & -\frac{1}{C_a} & 0 & 0 & 0 \\ 0 & \frac{1}{nC_1} & 0 & -\frac{1}{C_1 R_o} & -\frac{1}{C_1 R_o} \\ 0 & 0 & 0 & -\frac{1}{C_2 R_o} & -\frac{1}{C_2 R_o} \end{bmatrix} \begin{bmatrix} i_{Lb}(t) \\ i_{L\sigma}(t) \\ v_{ca}(t) \\ v_{c1}(t) \\ v_{c2}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_b} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_{fc}(t)] \quad (4.6)$$

Mode $\in \{(t_7 < t < t_8)\}$: During this mode the clamp capacitance C_a is fully discharged and the primary current $i_{L\sigma}$ start to reduce lower than $2\overline{I_{Lb}}$. Like the mode $\{(t_3 < t < t_4)\}$, this mode is represent the charge/discharge interval of parasitic capacitances of the switches. The dynamic state-space equation for this mode is:

$$\begin{bmatrix} \frac{di_{Lb}(t)}{dt} \\ \frac{di_{L\sigma}(t)}{dt} \\ \frac{dv_{ca}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_b} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{nL_\sigma} & 0 \\ \frac{1}{C_a} & -\frac{1}{C_a} & 0 & 0 & 0 \\ 0 & \frac{1}{nC_1} & 0 & -\frac{1}{C_1 R_o} & -\frac{1}{C_1 R_o} \\ 0 & 0 & 0 & -\frac{1}{C_2 R_o} & -\frac{1}{C_2 R_o} \end{bmatrix} \begin{bmatrix} i_{Lb}(t) \\ i_{L\sigma}(t) \\ v_{ca}(t) \\ v_{c1}(t) \\ v_{c2}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_b} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_{fc}(t)] \quad (4.7)$$

The dynamic state-space equations for states 9 to 16 are similar to equations (4.2) to (4.7) only differ in the way that C_1 and C_2 are charged.

4.2.2 Derivation of State-Space Averaging Model

In this section the averaged state equations over one switching cycle of the state variables i_{Lb}, v_{ca} and v_o have been derived.

Using the state-space dynamic equations (4.2) and (4.4) to (4.7), the low–frequency average input current $\langle i_{Lb}(t)\rangle_{T_s}$ over switching cycle can be given as (see Appendix C):

$$\frac{d\langle i_{Lb}(t)\rangle_{T_s}}{dt} = \frac{1}{2L_b}\Big((\langle v_{fc}(t)\rangle_{T_s})d_1(t) + (\langle v_{fc}(t)\rangle_{T_s} - \langle v_{ca}(t)\rangle_{T_s})d_1'(t) + (\langle v_{fc}(t)\rangle_{T_s})d_2(t) + (\langle v_{fc}(t)\rangle_{T_s} - \langle v_{ca}(t)\rangle_{T_s})d_2'(t)\Big) \tag{4.8}$$

where $\langle v_{fc}(t)\rangle_{T_s}$ and $\langle v_{ca}(t)\rangle_{T_s}$ are the low–frequency averaged values of the state variables v_{fc} and v_{ca}.

As shown in Fig. 4.1, the duty cycle $d(t)$ and its complementary $d'(t)$, which includes the charge and discharge period of parasitic capacitances, can be defined as:

$$d(t) = \frac{d_1(t)}{2} + \frac{d_2(t)}{2} \tag{4.9}$$

$$d'(t) = \frac{d_1'(t)}{2} + \frac{d_2'(t)}{2} \tag{4.10}$$

and $d(t)+d'(t) = 1$

Using (4.9) and (4.10), (4.8) can be simplified to:

$$\frac{d\langle i_{Lb}(t)\rangle_{T_s}}{dt} = \frac{1}{L_b}\Big(\langle v_{fc}(t)\rangle_{T_s} - \langle v_{ca}(t)\rangle_{T_s}d'(t)\Big) \tag{4.11}$$

Based on the converter operation (see Fig. 3.3) and using (4.2) and (4.4) to (4.7), the low–frequency averaged value of the clamp capacitor voltage over one cycle $\langle v_{ca}(t)\rangle_{T_s}$ is obtained as:

$$\frac{d\langle v_{ca}(t)\rangle_{T_s}}{dt} = \frac{1}{C_a}\left(\langle i_{Lb}(t)\rangle_{T_s} - \langle\left|i_{L\sigma}^{SH}(t)\right|\rangle_{T_s}\right)d'(t) \tag{4.12}$$

According to Fig. 3.5, the average primary current $\langle\left|i_{L\sigma}^{SH}(t)\right|\rangle_{T_s}$ for the shaded area A_{SH} over one cycle is given by:

$$\langle\left|i_{L\sigma}^{SH}(t)\right|\rangle_{T_s} = \frac{1}{2} I_p d'(t) \tag{4.13}$$

Referring to Fig. 3.5 (primary current waveform), the peak current I_p is obtained as

$$I_p = \frac{T_s}{L_\sigma}\left(\langle v_{ca}(t)\rangle_{T_s} - \frac{\langle v_o(t)\rangle_{T_s}}{2n}\right)d'(t) \tag{4.14}$$

Substituting of (4.14) in (4.13) and then substitute the result in (4.12), the average clamp capacitor voltage over T_s can be obtained as:

$$\begin{aligned}\frac{d\langle v_{ca}(t)\rangle_{T_s}}{dt} = \Bigg(&\frac{\langle i_{Lb}(t)\rangle_{T_s}}{C_a}d'(t) \\ &- \frac{T_s}{2C_aL_\sigma}\left(\langle v_{ca}(t)\rangle_{T_s} - \frac{\langle v_o(t)\rangle_{T_s}}{2n}\right)\left(d'(t)\right)^2\Bigg)\end{aligned} \tag{4.15}$$

Assuming that the voltages across the voltage–doubler capacitors are equal (i.e. $v_{C1}(t) = v_{C2}(t)$, see assumptions in Section 3.2.1), alternatively the average output voltage $\langle v_o(t)\rangle_{T_s}$ over one cycle is:

$$\frac{d\langle v_o(t)\rangle_{T_s}}{dt} = \frac{2}{nCT_s}\int_0^{T_s}|i_{L\sigma}(t)|dt - \frac{\langle v_o(t)\rangle_{T_s}}{R_o} \tag{4.16}$$

where $C = C_1 = C_2$.

From Fig. 3.5, it can be seen that the absolute value of the average primary current $\langle|i_{L\sigma}(t)|\rangle_{T_s}$ is equal to:

$$\begin{aligned}\langle|i_{L\sigma}(t)|\rangle_{T_s} &= \frac{1}{T_s}\int_0^{T_s} i_{L\sigma}(t)dt \\ &= \frac{1}{T_s}\left\{\frac{I_p}{2}\left(\frac{d_1'(t)}{2} + \frac{\delta_2(t)}{2}\right)T_s + \frac{I_p}{2}\left(\frac{d_2'(t)}{2} + \frac{\delta_1(t)}{2}\right)T_s\right\}\end{aligned} \tag{4.17}$$

where the fraction of the period $\delta(t)$ during which the energy stored in the leakage inductance is transferred to the secondary side over one cycle can be defined as[1]:

$$\delta(t) = \frac{\delta_1(t)}{2} + \frac{\delta_2(t)}{2} \tag{4.18}$$

Using (4.10) and (4.18), (4.17) can be simplified to:

$$\langle|i_{L\sigma}(t)|\rangle_{T_s} = \frac{I_p}{2}\left(d'(t) + \delta(t)\right) \tag{4.19}$$

where $I_p = 2\langle i_{Lb}(t)\rangle_{T_s}$ (see Section 3.2.2)

Substitution of (4.19) in (4.16) yields:

$$\frac{d\langle v_o(t)\rangle_{T_s}}{dt} = 2\left(\frac{\langle i_{Lb}(t)\rangle_{T_s}d'(t) + \langle i_{Lb}(t)\rangle_{T_s}\delta(t)}{nC} - \frac{\langle v_o(t)\rangle_{T_s}}{CR_o}\right) \tag{4.20}$$

From (4.11), (4.15), and (4.20) the small-signal model, the AC equivalent circuit and the small-signal transfer functions can be derived as described in the next sections.

[1]Referring to Fig. 4.1, $\delta(t)$ represents the total period of the modes (t_o,t_1), (t_1,t_2), (t_8,t_9), and (t_9,t_{10}) over T_s.

4.2.3 Small-Signal Model and AC Equivalent Circuit Derivation

To obtain the final linearized state equation that represents the dynamic behaviour of the converter, the nonlinear equations (4.11), (4.15), and (4.20) are extended around the quiescent operating point and then the DC and high order terms are neglected [105]. This is achieved by introducing small perturbations around nominal operating point as shown in Table 4.1.

TABLE 4.1
PERTURBATION STATE VALUES

$\langle v_{Lb}(t)\rangle_{T_s} = V_{Lb} + \hat{v}_{Lb}(t)$	$\delta(t) = \Delta + \hat{\delta}(t)$
$\langle v_{fc}(t)\rangle_{T_s} = V_{fc} + \hat{v}_{fc}(t)$	$d'(t) = D' - \hat{d}(t)$
$\langle v_{ca}(t)\rangle_{T_s} = V_{ca} + \hat{v}_{ca}(t)$	$\langle i_{Lb}(t)\rangle_{T_s} = I_{Lb} + \hat{i}_{Lb}(t)$
$\langle v_{L\sigma}(t)\rangle_{T_s} = V_{L\sigma} + \hat{v}_{L\sigma}(t)$	$\langle i_{L\sigma}(t)\rangle_{T_s} = I_{L\sigma} + \hat{i}_{L\sigma}(t)$
$\langle v_o(t)\rangle_{T_s} = V_o + \hat{v}_o(t)$	$\langle i_{ca}(t)\rangle_{T_s} = I_{ca} + \hat{i}_{ca}(t)$
$d(t) = D + \hat{d}(t)$	

Applying this to the non–linear equations, the following state-space equation is obtained for the small-signal relations:

$$\begin{bmatrix} L_b & 0 & 0 \\ 0 & C_a & 0 \\ 0 & 0 & \frac{C}{2} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \hat{i}_{Lb}(t) \\ \hat{v}_{Ca}(t) \\ \hat{v}_o(t) \end{bmatrix} = \begin{bmatrix} 0 & -D' & 0 \\ D' & -g_3 & g_2 \\ J & p_3 & -p_4 \end{bmatrix} \times \begin{bmatrix} \hat{i}_{Lb}(t) \\ \hat{v}_{Ca}(t) \\ \hat{v}_o(t) \end{bmatrix} + \begin{bmatrix} V_{Ca} \\ g_1 \\ -p_1 \end{bmatrix} \hat{d}(t) + \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \hat{v}_{fc}(t) \tag{4.21}$$

where the coefficients of (4.21) are defined in Table 4.2.

TABLE 4.2
COEFFICIENTS OF AC EQUIVALENT CIRCUIT

$g_1 = \left(\frac{T_s D'}{L_\sigma}\left(V_{Ca} - \frac{V_o}{2n}\right) - I_{Lb}\right)$	$p_1 = \frac{2I_{Lb}V_{Ca}}{V_o}$
$g_2 = \frac{T_s (D')^2}{4nL_\sigma}$	$p_2 = \frac{I_{Lb}}{nV_o}(D' + \Delta)$
$g_3 = \frac{(D')^2}{2L_\sigma f_s}$	$p_3 = \frac{2I_{Lb}D'}{V_o}$
$J = \frac{(D' + \Delta)}{n}$	$p_4 = \frac{I_{Lb}}{nV_o}(D' + \Delta) + \frac{1}{R_o}$

Note that the state $\hat{\delta}(t)$ has been eliminated from (4.21) by the following substitution (see Appendix E):

$$\hat{\delta}(t) = \frac{2nD'}{V_o}\hat{v}_{Ca}(t) - \left(\frac{D'}{V_o} + \frac{\Delta}{V_o}\right)\hat{v}_o(t) - \frac{2n}{V_o}\left(V_{Ca} - \frac{V_o}{2n}\right)\hat{d}(t) \qquad (4.22)$$

where Δ and D' are defined in (3.18) and (3.23) respectively.

The state-space equation of (4.21) can be represented by the AC equivalent circuit in Fig. 4.2, where the FC voltage $\hat{v}_{fc}(t)$ can be represented as $(\hat{v}_{fc\_o}(t) - \hat{i}_{Lb}(t)R_{fc})$ based on the FC model described in Section 2.2.2.

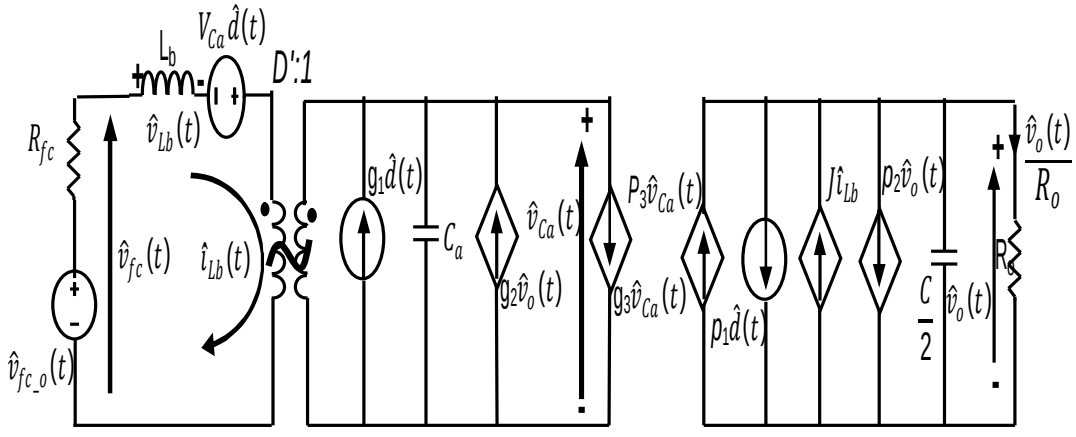


Fig. 4.2 Small signal AC equivalent model of the proposed FBCFC

It can be seen that the developed dynamic model of the FC converter system takes into account all features, including the FC output characteristics, the active clamp circuit, and voltage–doubler circuit, and the parasitic elements.

4.3 Controller Design and Analysis

Since the proposed converter is a non-minimum phase system, therefore it is exhibits a RHPZ[2] (see Section A-). If a direct duty cycle control is used to regulate the output voltage, the RHPZ would limit the available bandwidth for stable operation of the converter. Therefore, direct duty cycle control for the converter is first discussed in this section, after which to eliminate the impact of the RHPZ on the stable operation of the converter, a two-loop current mode controller is designed and analysed.

4.3.1 Direct Duty Cycle Control

4.3.2.1 Small-Signal Characteristics of Direct Duty Cycle Open-Loop Converter

By performing Laplace transform on (4.21) the following state-space equation in s-domain is obtained:

$$\begin{bmatrix} s.L_b & D' & 0 \\ -D' & s.C_a + g_3 & -g_2 \\ -J & -p_3 & s.\frac{C}{2} + p_4 \end{bmatrix} . \begin{bmatrix} \hat{i}_{Lb}(s) \\ \hat{v}_{Ca}(s) \\ \hat{v}_o(s) \end{bmatrix} = \begin{bmatrix} V_{Ca} \\ g_1 \\ -p_1 \end{bmatrix} . [\hat{d}(s)] + \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} [\hat{v}_{fc}(s)] \qquad (4.23)$$

Using (4.23), a number of small-signal transfer functions can be derived that provide important information about the dynamic behaviour of the proposed converter, as shown below.

[2] The RHPZ is a common feature of all CFCs

A- Control-to-Output Transfer Function

One of the important transfer functions to study the dynamic performance of the converter and to design an appropriate system controller (see Section 4.3.2) is the control-to-output voltage transfer function $G_{vd}(s)$. This transfer function can be derived from (4.23) and written as (see Appendix D):

$$G_{vd}(s) = \left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{\hat{v}_{fc}(s)=0} = G_{go}\frac{m_1 s^2 + m_2 s + 1}{q_1 s^3 + q_2 s^2 + q_3 s + 1} \qquad (4.24)$$

The full expressions for the numerator and denominator coefficients of (4.24) are shown in Table 4.3.

TABLE 4.3
COEFFICIENTS OF THE CONTROL-TO-OUTPUT VOLTAGE TRANSFER FUNCTION

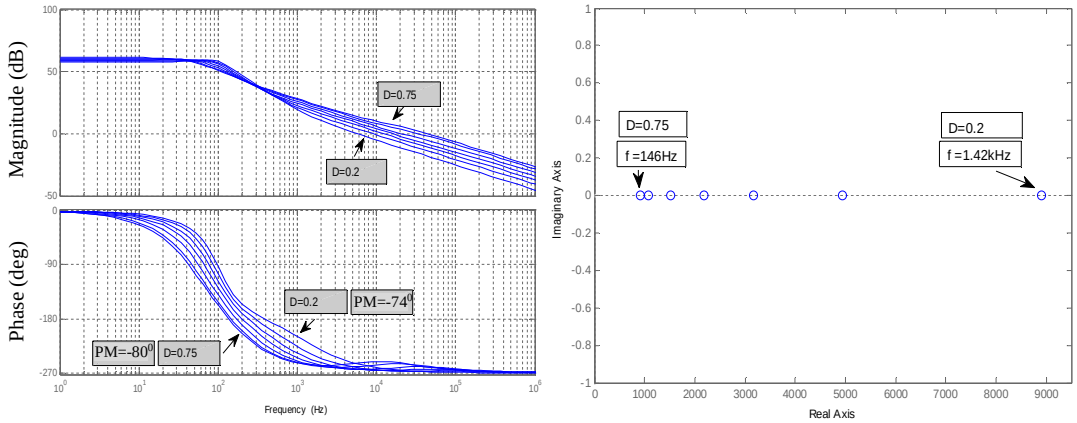
$G_{g0} = \frac{-p_1 D'^2 + Jg_3 V_{Ca} - JD'g_1 + p_3 V_{Ca} D'}{p_2 D'^2 + Jg_2 D'}$	$q_1 = \frac{L_b . C . C_a}{2p_2 D'^2 + 2Jg_2 D'}$
$m_1 = \frac{-L_b . C_a . p_1}{-p_1 D'^2 + Jg_3 V_{Ca} - JD'g_1 + p_3 V_{Ca} D'}$	$q_2 = \frac{L_b . C . g_3 + 2C_a L p_2}{2p_2 D'^2 + 2Jg_2 D'}$
$m_2 = \frac{C_a J V_{Ca} - g_3 p_1 L_b + p_3 g_1 L_b}{-p_1 D'^2 + Jg_3 V_{Ca} - JD'g_1 + p_3 V_{Ca} D'}$	$q_3 = \frac{(D')^2 C - 2g_2 p_3 L_b + 2p_2 g_3 L_b}{2p_2 (D')^2 + 2Jg_2 D'}$

Using the conditions and parameter values listed in Table 4.4, the transfer function $G_{vd}(s)$ has been evaluated for a range of duty cycle values.

TABLE 4.4
PARAMETER VALUES USED TO EVALUATE THE CONVERTER

Parameters	Values	Parameters	Values
Output Power (P_o)	418 W	Switching Frequency (f_s)	20kHz
FC Voltage (v_{fc})	38V	Output Capacitor (C)	500 µF
FC Resistance (R_{fc})	0.35Ω	Boost Inductance (L_b)	475µH
Load Resistance (R_o)	973Ω	Clamp Capacitance (C_a)	10 µF
Output Voltage (V_o)	650V	Transformer Turns Ratio (n)	7.4

The results are shown in Fig. 4.3a in the form of Bode plots, where it can be seen that the magnitude plot doesn't exhibit any resonant peak(s). However, the phase plot shows a phase shift of more than 180^0. This is due to the presence of a RHPZ, similar to that found for the conventional current-fed boost converter, which adds an extra 180^0 phase lag. Also, it can be seen from Fig. 4.3b that the frequency of the RHPZ varies with the duty cycle and/or the load condition, and the minimum frequency of the RHPZ occurs at high-load. Therefore, to ensure an appropriate stability margin for the converter system, the converter voltage control must be designed with this condition in mind (see Section 4.5).



(a) (b)

Fig. 4.3 Dynamic performance of the proposed converter as a function of duty cycle: (a) Bode plots of $G_{vd}(s)$, (b) RHPZ map of $G_{vd}(s)$.

B- Input Voltage-to-Output Transfer Function

To evaluate the impact of low-frequency disturbances in the FC voltage on the DC link voltage regulation, a small-signal input voltage-to-output voltage transfer function is obtained from (4.23) and can be written in the form:

$$G_{v_{fc}v}(s) = \left.\frac{\hat{v}_o(s)}{\hat{v}_{fc}(s)}\right|_{\hat{d}(s)=0} = G_{fc}\frac{as+1}{q_1 s^3 + q_2 s^2 + q_3 s + 1} \qquad (4.25)$$

where the coefficients of (4.25) are given in Table 4.3 and below

$$a = \frac{JC_a}{(Jg_3 + p_3D')} \tag{4.26}$$

$$G_{fc} = \frac{(Jg_3 + p_3D')}{(p_2D^2 + Jg_2D')} \tag{4.27}$$

As shown in the Bode plot of Fig. 4.4, the converter has the ablity to reject peturbation in the FC voltage for frequencies above 100 rad/s.

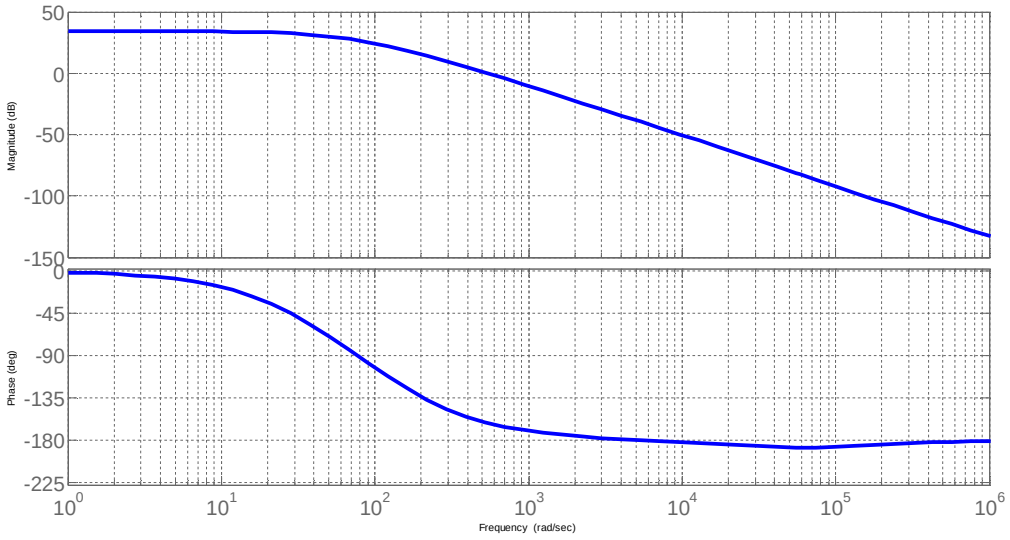


Fig. 4.4 Bode plot of the FC voltage-to-output small-signal transfer function $G_{v_{fc}v}(s)$

4.3.2 Current–Mode Control

As indicated in Section A-, RHPZ limits the available bandwidth for the converter resulting in a slower dynamic response for the converter. Different techniques can be used to eliminate a RHPZ or to increase the RHPZ frequency in order to speed up the response of the system [67, 68]. Most of these techniques make the input current discontinuous, which is not acceptable for a FC source. For that reason, a two loop controller, as shown in Fig. 4.5 is used to eliminate the RHPZ from the closed-loop

characteristic. It simplifies the design of the control loop compensators, increases the bandwidth, and can also be used to limit the maximum output current of FC.

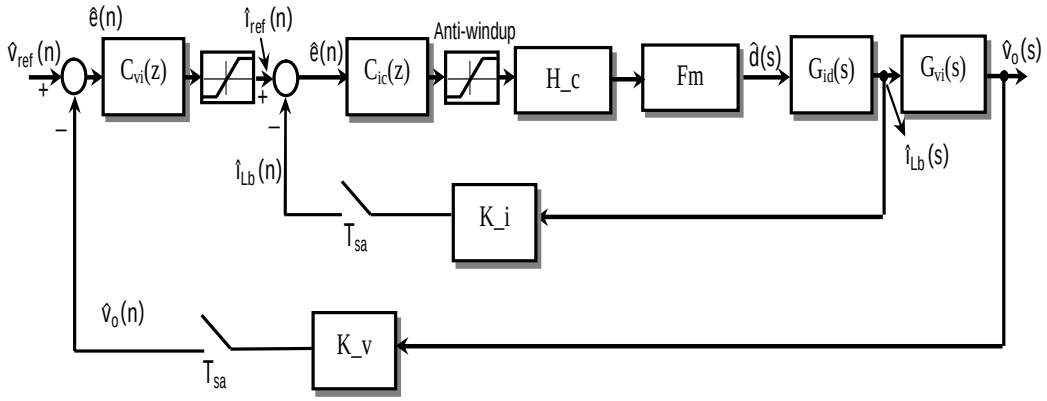


Fig. 4.5 Small-signal block digram of two loop current mode control

However, since the dynamic response of the FC is slow, the converter controller should be designed with an appropriate bandwidth give enough time for the FC to recover to it is steady-state condition. It was shown in Section 2.2 that the FC takes about 0.24sec (i.e. the characteristic dynamic frequency of the FC is about 0.66Hz[3]) to change from the no-load state to the full-load state. Thus, even for the lowest frequency of the RHPZ (146Hz), shown in Fig. 4.3b at D = 0.75, a sufficient frequency range is available to design the desired bandwidth for the voltage loop controller of the FC control system.

A two–loop controller can be implemented either in an analogue or digital environment. However, for power electronic DC-DC converters, digital control using a DSP or microcontroller is becoming more and more common because of increased flexibility, lower susceptibility to environmental variations and lower EMI vulnerability compared to analogue control [106]. Several digital control techniques have been proposed for DC-DC converter systems, such as digital average current mode controller and predictive current controller (PCC) techniques [107-109].

[3] The FC dynamic frequency (f_{FC}) is equal to ($1/2\pi\ \tau_{FC}$), where τ_{FC} is the FC time constant equal to 0.24s.

As stated earlier, the FC needs about 0.24 second (as a time constant) to respond after a sudden load applied across it from the no-load status. Therefore, it is unnecessary to use a fast control technique like PCC, because of the time taken by the FC to recover to its steady state condition. Based on that, digital average current-mode controller has been selected for control of the proposed FC converter system without the need for a complex computational algorithm.

4.3.2.1 Selection of the Parameters of Current Mode Control

To obtain the required control parameters, the control system has been designed systematically based on the dynamic model developed in Section 4.2.

As shown in Fig. 4.5, the developed digital average current–mode controller consists of inner and outer loop controllers with two digital PI compensators ($C_{id}(z)$ and $C_{vi}(z)$). Each compensator has an anti-windup protection system. The digital PI controllers are designed based on the "digital redesign approach" so that the controller is designed initially in the s-domain and is then discretized in the z-domain using the Backward Euler method [110]. The design parameters of the proposed converter are given in Table 4.5.

TABLE 4.5
CIRCUIT PARAMETER VALUES

Parameter	Value	Parameter	Value
Output Power (P_o)	0.1~1.2kW	Leakage Inductance (L_σ)	2 µH
Fuel Cell Voltage (v_{fc})	26~43V	Output Capacitor ($C=C_1=C_2$)	500µF
Load Resistance (R_o)	352~4225Ω	Duty Cycle (D)	0.01~0.8
Output Voltage (V_o)	650V	Boost Inductance (L_b)	475µH
Transformer Turns Ratio (n)	7.4	Clamp Capacitance (C_a)	10µF
Switching Frequency (f_s)	20kHz	FC Resistance (R_{fc})	0.35Ω

Using Fig. 4.5, the input current and output voltage open loop transfer functions $T_i(s)$

and $T_v(s)$ are obtained as:

$$T_i(s) = H_c H_{smp} G_{id}(s) C_{id}(s) F_m K\_i \tag{4.28}$$

$$T_v(s) = H_{smp} G_{vi}(s) C_{vi}(s) K\_v \tag{4.29}$$

where H_{smp} and H_c are the sampling delay and the computation delay respectively due to ADC sampling and calculation time of the DSP. Their transfer functions are shown below:

$$H_{smp} = \frac{1 - e^{-T_{sa}}}{s} \tag{4.30}$$

$$H_c = e^{-T_d} \tag{4.31}$$

where T_{sa} is the sampling time and T_d is the computational delay time between the ADC sampling instant and the duty cycle update.

4.3.2.2 Compensator Design of Current Mode Control

Based on the state-space equation in (4.23), the control-to-input current transfer function $G_{id}(s)$ can be obtained by setting $\hat{v}_{fc}(s)$ and $\hat{v}_o(s)$ equal to zero. This yield:

$$G_{id}(s) = \frac{\hat{i}_{Lb}(s)}{\hat{d}(s)}\bigg|_{\hat{v}_{fc}(s),\hat{v}_o(s)=0} = G_{io}\frac{a_o s + 1}{b_1 s^2 + b_2 s + 1} \tag{4.32}$$

where the coefficients are given by the expressions in Table 4.6.

TABLE 4.6
COEFFICIENTS OF THE GID(S) AND GVI(S) TRANSFER FUNCTIONS

Parameters	Values	Parameters	Values
G_{io}	$\frac{g_3 V_{Ca} - g_1 D'}{(1-D)^2}$	b_2	$\frac{g_3 L_b}{(1-D)^2}$
a_o	$\frac{C_a V_{Ca}}{(g_3 V_{Ca} - g_1 D')}$	G_{vo}	JR_o
b_1	$\frac{C_a L_b}{(1-D)^2}$	β	$\frac{CR_o}{2}$

Since the slew rate of boost inductor current is significantly higher than the rate of $\hat{i}_{ref}(n)$, the outer-voltage loop controller is designed for a bandwidth much smaller than inner-current loop controller. Therefore, the current-to-output voltage transfer function $G_{vi}(s)$ can be derived by setting $\hat{d}(s)$ and $\hat{v}_{fc}(s)$ in (4.23) equal to zero, which yields:

$$G_{vi}(s) = \left.\frac{\hat{v}_o(s)}{\hat{i}_{Lb}(s)}\right|_{\hat{d}(s),\hat{v}_{fc}(s)=0} = G_{vo}\frac{1}{\beta s + 1} \tag{4.33}$$

where the expressions for coefficients β and G_{vo} are given in Table 4.6.

By substituting the parameters of Table 4.5 in (4.32) and (4.33), the following expressions for $G_{id}(s)$ and $G_{vi}(s)$ are obtained:

$$G_{id}(s) = 599.7587\frac{2.468e^{-6}s+1}{1.515e^{-8}s^2+0.005938\,s+1} \tag{4.34}$$

$$G_{vi}(s) = 28.1664\frac{1}{0.176s+1} \tag{4.35}$$

If the digitized sensed output voltage $v_o(n)$ in Fig. 4.5 is designed to be equal to the maximum output voltage V_{omax} then voltage sensing gain $K_{\_v}$ will be equal to 1. In a similar manner the current sensing gain $K_{\_i}$ can be scaled to be equal to 1, where $K_{\_v}$ and $K_{\_i}$ are representing the total gains between the plant outputs and the ADC converter outputs. This can be done by scaling the digitized sensed output voltage and input current in software in the DSP (see Section 4.5.2).

By configuring the software together with the DSP on-chip PWM hardware such that the output d(n) of the PWM modulator F_m, shown in Fig. 4.5, is equal to 100% when the input controller signal (U(n)) is a maximum, then F_m will be equal to 1. This is so since:

$$F_m = \frac{d(n)}{U(n)} \tag{4.36}$$

For the outer voltage loop and inner current loop the PI compensator equations are given by

$$C_{vi}(s) = K_{pv} + \frac{K_{iv}}{s} \tag{4.37}$$

$$C_{id}(s) = K_{pc} + \frac{K_{ic}}{s} \tag{4.38}$$

The cross-over frequency ω_c of the open loop transfer function $T_i(s)$ for the inner current loop is selected as about one tenth of ω_s and is equal to 1.25×10^4 rad/s, while the cross-over frequency for $T_v(s)$ is selected to be about one fifth of that of the frequency of the RHPZ and is equal to 200 rad/s at full-load state[4]. The sampling time is chosen as T_{sa} = 50μs and the computational delay time is assumed to be $T_d = 0.25T_{sa}$ respectively[5].

To design the PI compensators with the desired phase margin (PM) at the above cross-over frequencies, the Control Toolbox in Matlab was used [111]. The corresponding parameters of the PI compensators can be imported automatically, which are found as:

$$C_{vi}(s) = K_{pv} + \frac{K_{iv}}{s} = 1.08625 + \frac{100.748}{s} \tag{4.39}$$

$$C_{id}(s) = K_{pc} + \frac{K_{ic}}{s} = 0.1147 + \frac{506.66}{s} \tag{4.40}$$

The Bode plots of the uncompensated and compensated open current loop system are shown in Fig. 4.6. It can be seen that as desired the phase margin at $\omega_c = 1.23\times10^4$ rad/s is enhanced to 71^0.

[4] The selected bandwidth of the inner and outer loop has been based on the worst case, which is the full load condition.

[5] As shown in Section 4.6.4 to avoid noises at ON and OFF transitions, the sampling time is selected equal to the PWM period. Hence, $T_{sa} = 1/f_s$. The computational delay time is between the ADC sampling instant and the PWM duty cycle update, Hence, $T_d=0.5T_{sa}$, for worse case T_d has been assumed equal to $0.25T_{sa}$.

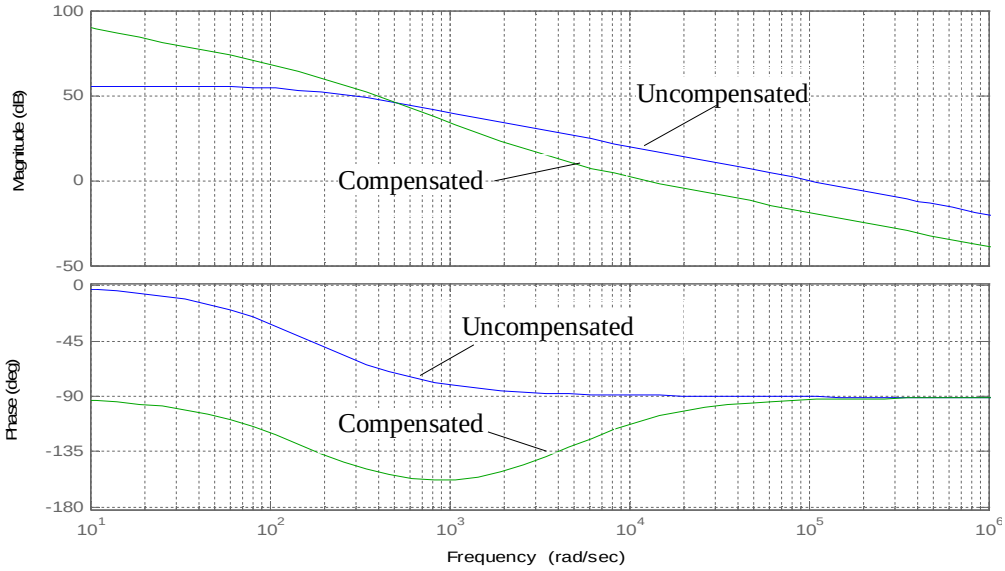


Fig. 4.6 Bode plot of uncompensated and compensated open loop current controller

Fig. 4.7 shows the Bode plots of the uncompensated and compensated open voltage loop controller. The phase margin is also improved to 66^0 at the desired cross-over frequency equal to 193 rad/s.

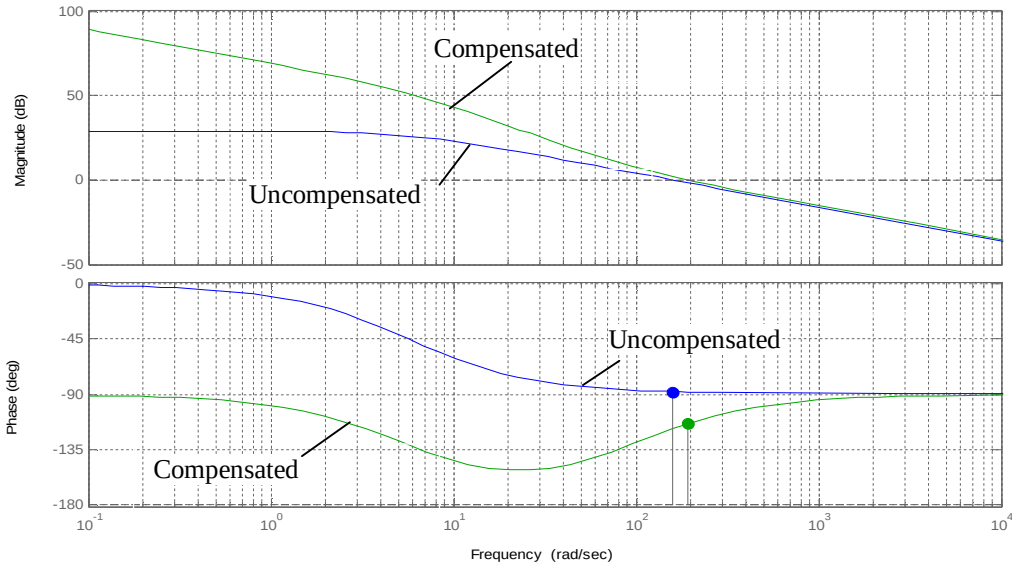


Fig. 4.7 Bode plot of uncompensated and compensated open loop voltage controller

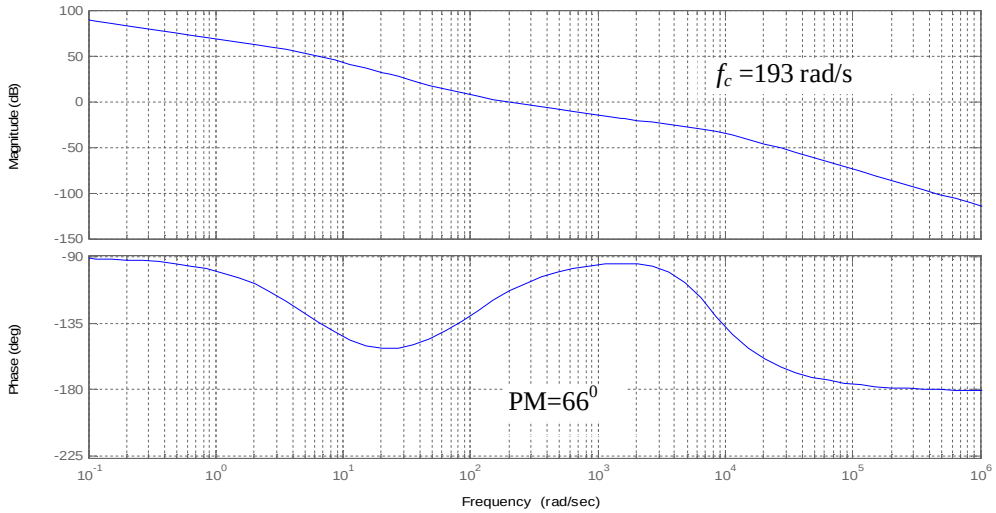


Fig. 4.8 Bode plot of an overall compensated open loop system

Fig. 4.8 shows the total open loop response of the system, with the desired bandwidth 193 rad/s and a phase margin 66^0.

As mentioned earlier, digital PI controllers are designed using Backward Euler approache. Hence, the proportional (K_{ov}, K_{oc}) and integral (K_{qv}, K_{qc}) parameters of the digital PI controllers for the voltage and current loop respectively can be expressed as following [110]: $K_{ov} = K_{pv}$, $K_{qv} = K_{iv}T_{sa}$, $K_{oc} = K_{pc}$, and $K_{qc} = K_{ic}T_{sa}$, where the parameter for the anti-windup correction is selected as $K_{corr}= K_q/ K_o$ for both PI controllers.

4.4 Comparison of Dynamic Performance of the Proposed CFC with Other FBCFC Topologies

The steady-state analysis of the proposed converter under different load conditions in Chapter 3 has shown that the converter outperforms other competing CFC configurations in terms of efficiency, input current ripple, voltage rating of the semiconductor devices, and component utilisation (see. Fig. 3.39, Fig. 3.42, and Fig. 3.45).

In this section the comparison has been extended to evaluate the dynamic performance of the converter compared to two other competing CFC, namely that of a Config.2 (see Fig. 2.26) and Config.3 (see Fig. 2.29c). The comparison is based on the control-to-output voltage transfer function $G_{vd}(s)$ of each configuration for a specific load condition[6].

The comparison has been made for all compared configurations using the same parameters shown in Table 4.4 expect that: n = 8.85 and C=1100 µF have been used for Config.3.

4.4.1 FBCFC with Voltage–Doubler Rectifier Diode without Active–Clamp Circuit (Config.2)

The pole-zero maps and the Bode plots of the control-to-output transfer function for Config.2 and the proposed converter are compared in Fig. 4.9 and Fig. 4.10 respectively. As a worst case for the controller parameters design, the comparison has been made at full-load condition. They show that the poles and zeros of Config.2 are at ρ_{12}=-4.24±j102 and $z_1=1.21\times10^3$ with a resonant frequency of ω_n=102 rad/s and a damping ratio ξ=0.0417. This compares with the poles and zeros of the proposed converter at ρ_1=-42.8, ρ_2=-137, $\rho_3=-4.98\times10^4$, z_1=543, and $z_2=-2.4\times10^4$ with damping ratio ξ =1. As shown in Fig. 4.9[7], instead of the three real poles of $G_{vd}(s)$ of the proposed converter, Config.2 has two resonant low frequency poles. Thus, this configuration exhibits a very lightly damped resonant at 16Hz which is absent in the proposed converter. The absence of resonant has a positive effect on the component ratings for the proposed converter and simplifies the design of a voltage controller (see

[6] The control-to-output transfer function of the proposed converter has been derived in (4.24), while the transfer functions for the other CFC configurations are shown in Appendix D.
[7] Also it is worth mentioning that the pair ρ_3 and z_2 are nearly cancels at this load condition.

Section 4.5).

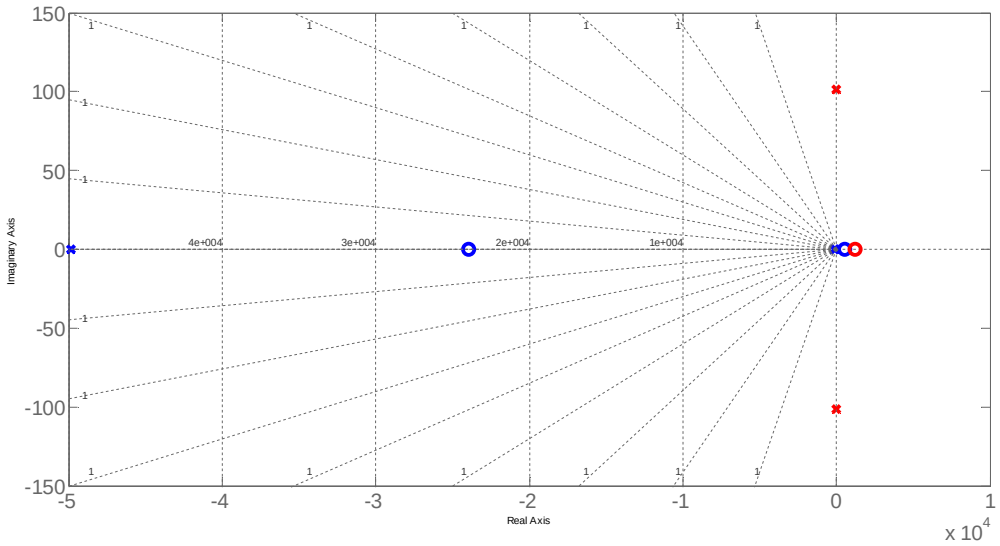


Fig. 4.9 Pole-zero maps of Config.2 (red) and the proposed CFC (blue)

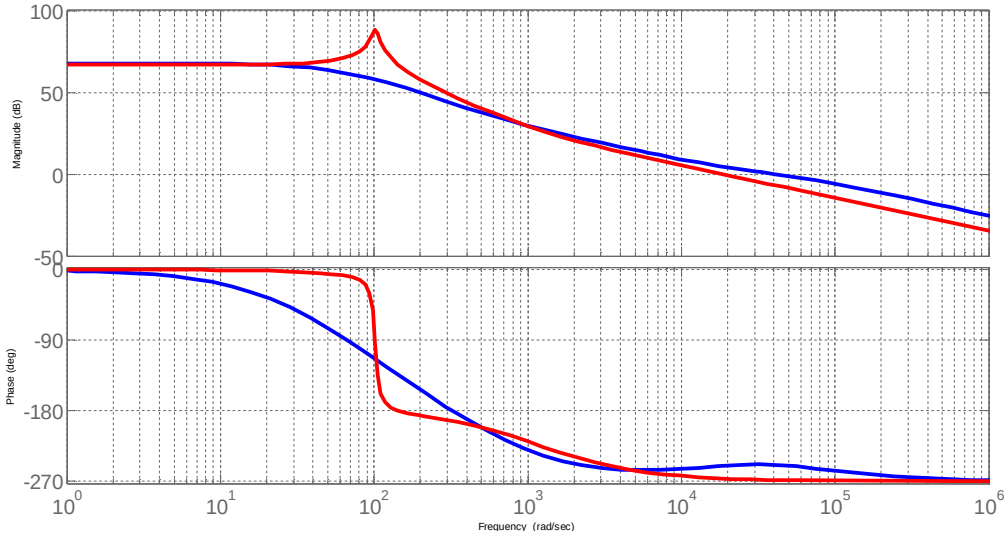


Fig. 4.10 Bode plots of the $G_{vd}(s)$ of Config.2 (red) and the proposed CFC (blue)

The small-signal transfer functions can vary with the load condition. Therefore, the dynamic performance of the proposed converter has also been evaluated at light load. The results for 35% load are depicted in Fig. 4.11, where it can be seen that when the load is reduced from 100% to 35%, the poles of Config.2 migrate from 16Hz to 32Hz with a further reduction in damping ratio (from $\xi = 0.0417$ to $\xi = 0.00816$). For the proposed converter the poles ρ_1 and ρ_2 migrate from the real axis to ρ_{12} =-86.4±j70.5

with a damping ratio of 0.775 and resonant frequency of (18Hz). Hence, at light load condition the proposed converter does exhibit an oscillatory behaviour, but this highly damped. This is in contrast to Config.2 which exhibit a virtually undamped resonant at light load, and would be unacceptable for a practical implementation.

Based on the above analysis, an active-clamp circuit not only clamps the voltage overshoot across the bridge switches but also improves the dynamic response of the CFC.

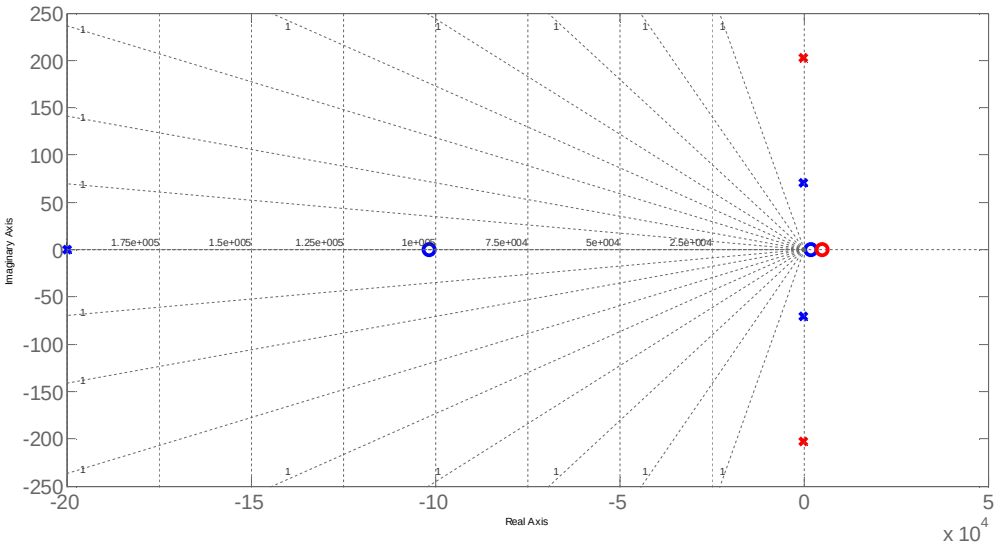


Fig. 4.11 Pole-zero maps of the $G_{vd}(s)$ of Config.2 (red) and the proposed CFC (blue) at light load

4.4.2 FBCFC with Active-Clamp Circuit (Config.3)

As stated in Section 4.4.1, the main improvement in the dynamic performance of the proposed converter in respect to Config.2 is due to the active-clamp circuit. However, as will be shown in this section, the proposed converter has another feature make it outperform another competing CFC configuration. This feature is evaluated by comparing the control-to-output voltage transfer function of the proposed converter in respect to that of Config.3.

The pole-zero maps of the two configurations at 35% of the full load are shown in Fig. 4.12. It can be seen that the poles of Config.3 has lower resonant frequency and damping ratio (10Hz, and 0.69 respectively), while these of the proposed converter are higher (19Hz, and 0.73 respectively). In addition, the Bode plot in Fig. 4.13 shows that the converter exhibits a higher cross-over frequency than one with Confg.3.

A smaller duty cycle, higher conversion ratio, and lower leakage inductance introduced by the proposed converter, results in the above positive effect. The result is that the proposed converter has a better dynamic behaviour.

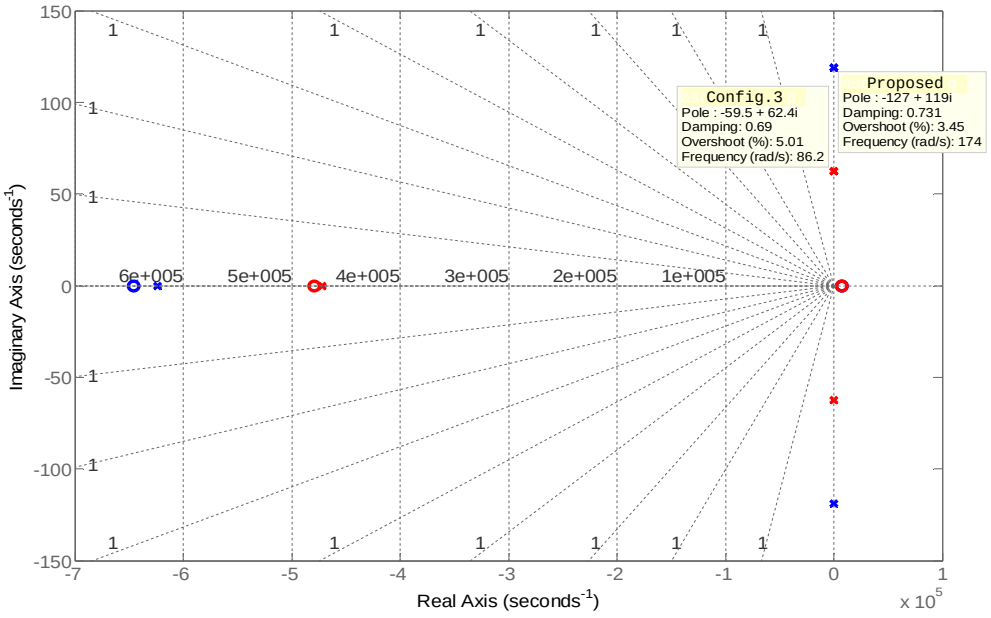


Fig. 4.12 Pole-zero maps of Config.3 (red) and the proposed CFC (blue) at $R_o = 900\Omega$

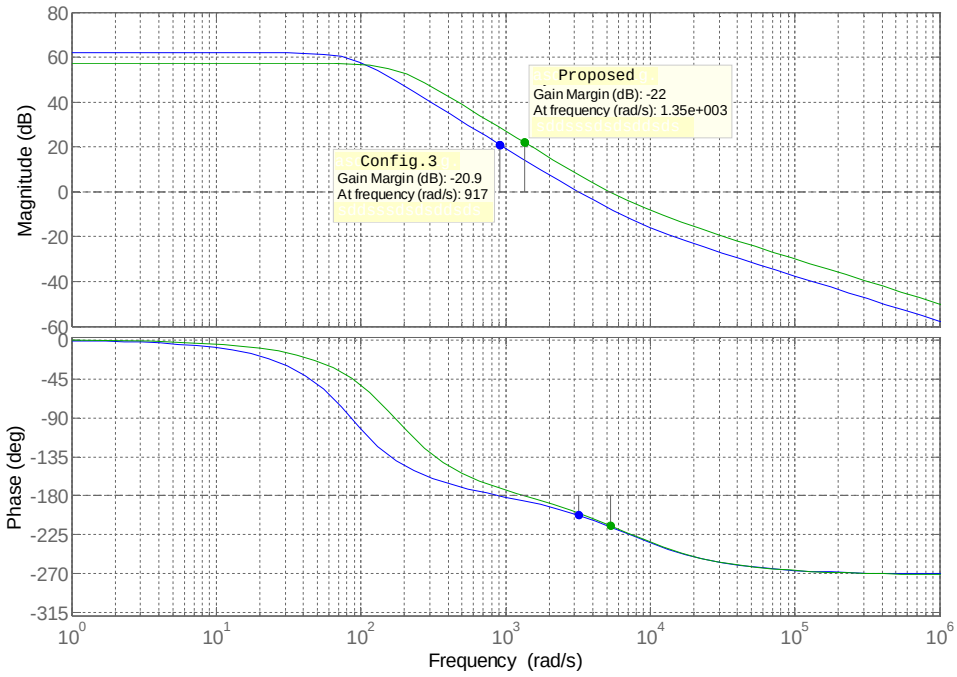


Fig. 4.13 Bode plots of Config.3 (blue) and the proposed CFC (green) at $R_o = 900\Omega$

4.5 Verification of Dynamic Model and Control System

To verify the validity of the mathematical model of the proposed converter incorporating the two–loop controller, two different approaches have been developed. The first approach describes the averaged behaviour of the converter with the two–loop controller, while a second approach has been developed to accurately evaluate the converter system performance with the two–loop controller.

4.5.1 Small-Signal Mathematical Model Approach

The first step taken to verify the dynamic model of the FC converter system is to simulate the developed small-signal transfer functions as a block diagram in the Simulink environment. The parameters of the small-signal transfer functions are chosen for the full load condition as shown in (4.34) and (4.35). Two digital PI compensators have been used and their parameters are tuned based on the controller design in Section

4.3.2. The dynamic performance of the converter is evaluated for load disturbance imposed by the Timer block in Fig. 4.14.

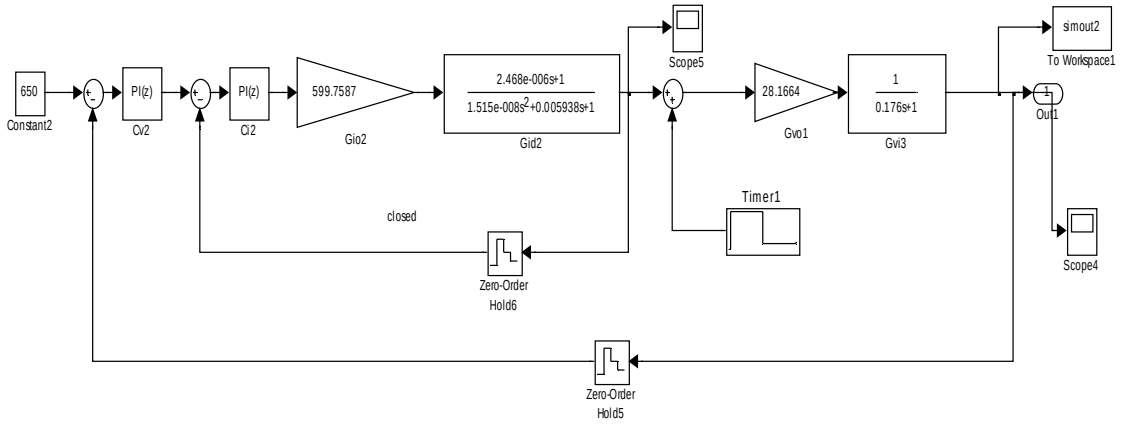


Fig. 4.14 Simulink block diagram based on developed small-signal transfer functions

Fig. 4.15 shows that the output voltage is regulated back to 650V in about 15ms when the power changes from 500W to 205W.

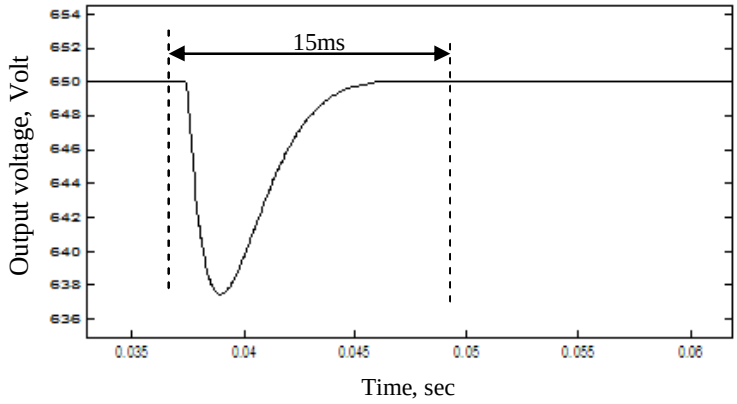


Fig. 4.15 Simulation results based on the small-signal mathematical model approach

Verifying the converter performance with the closed-loop control system by simulating the small-signal transfer functions significantly speeds up the simulation. However, it does not take into account the non-linear characteristics that are involved in the power electronic converter system. Thus, while this approach is helpful to give an indication of the performance for the converter the results may not be accurate over the entire load

range. Therefore, a further accurate analysis based on a physical components model (PCM) has been carried out in this work.

4.5.2 Physical Components Model Approach

The ability to trade off between model fidelity and simulation speed is a critical issue for an efficient development prior to the construction of a practical converter system. PCM at various levels of fidelity are necessary for the FC converter system to ensure that the final results are very close to reality. In addition, modelling of the converter system and the controller in a particular environment can ensure a high level of accuracy. The PSpice program is very suitable for simulating power electronic circuits that contain switching devices, non-linear transformers, and other non-linear components. But it is less suited for control system simulation because of potential convergence difficulties. Also, simulating the control system in PSpice may require a large amount of time for analysis. On the other hand, Matlab/Simulink is a very powerful program for control engineering, but it is less suitable for accurate modelling of power electronic circuit characteristics. Therefore, to get around this problem and accurately evaluate the converter performance with the control system, a new approach has been developed in this work based on integrating the PCM of the converter in PSpice with the controller in Simulink, using the SLPS integrated simulation platform (see reference [102] for more details about co-simulation environments).

The basic SLPS software architecture is depicted in Fig. 4.16. This architecture shows how the data exchange (sensor data and control signals) between the PCM in PSpice and the control system in Simulink is implemented.

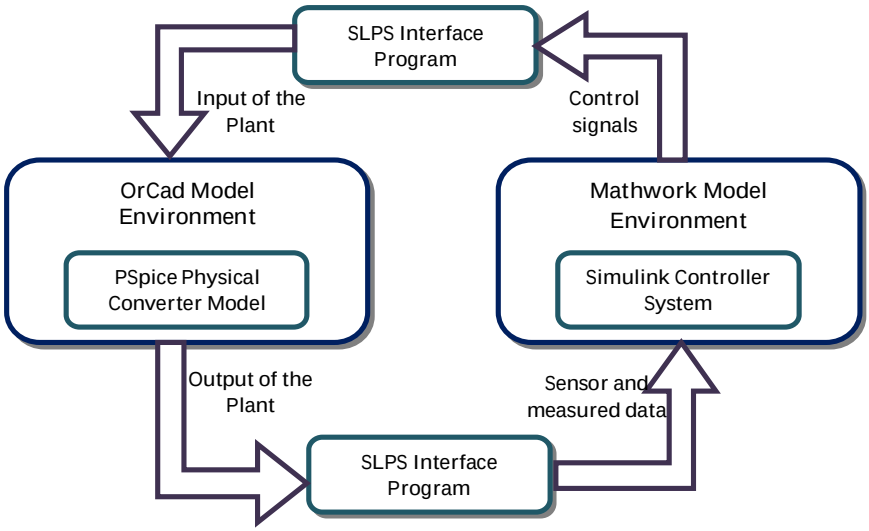


Fig. 4.16 SLPS integration software architecture

The complete model of the FC converter system with the digital controller structure is shown in Fig. 4.17, where it can be seen that the PCM of the converter (see Fig. 3.11) has been modelled in PSpice and embedded in the Simulink model, as a sub-circuit block via the SLPS software.

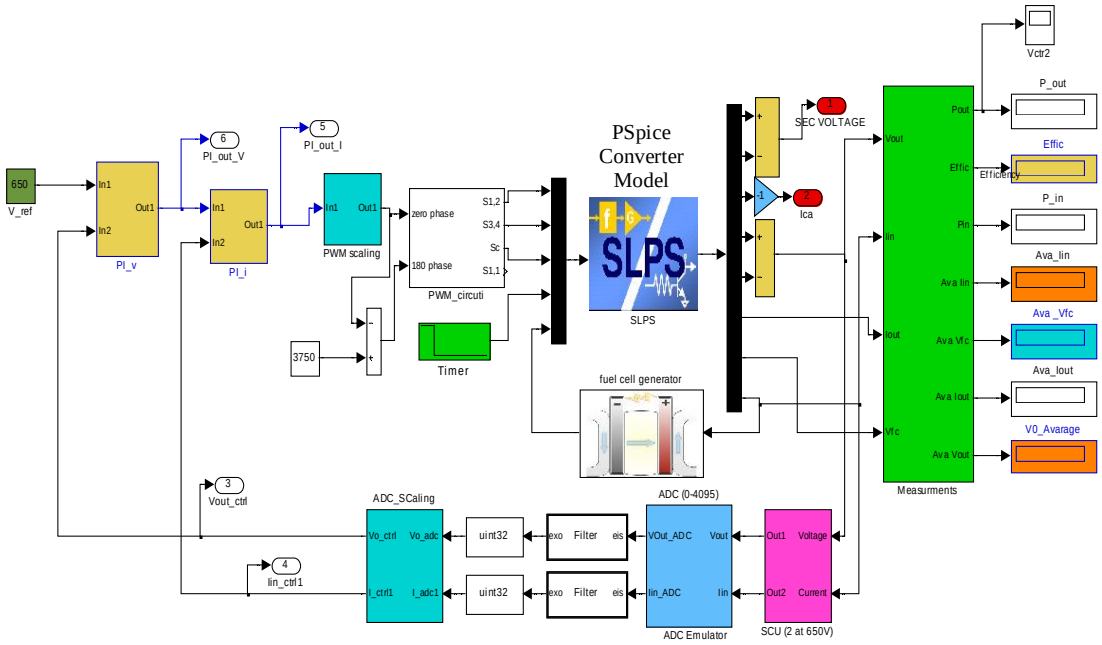


Fig. 4.17 Digital controller block diagram in Simulink integrated with the PCM of the converter via SLPS

Because the designed digital average current-mode controller has been implemented in a 32-bit fixed-point DSP processor (see Section 4.6), the on-chip ADC converter, PWM "compare function" and other functions have been emulated in Simulink, as shown in Fig. 4.17. A fixed-point data type has been utilised for the whole control system.

The measured output voltage and the FC current signals taken from the "SLPS" block are scaled and limited to 2.5V using the signal conditioning unit "SCU" block before being fed in to the "ADC emulator" block[8]. After that the measured signals have been digitized by a 12-bit "ADC emulator" (see Appendix G, Fig. G.1). The output of this unit is an unsigned integer number. To attenuate unwanted noise caused by the parasitic components (see Section 3.3.1 for more detail about this effect), the output of the "ADC emulator" block is followed by a moving average filters, as shown in Fig. 4.17.

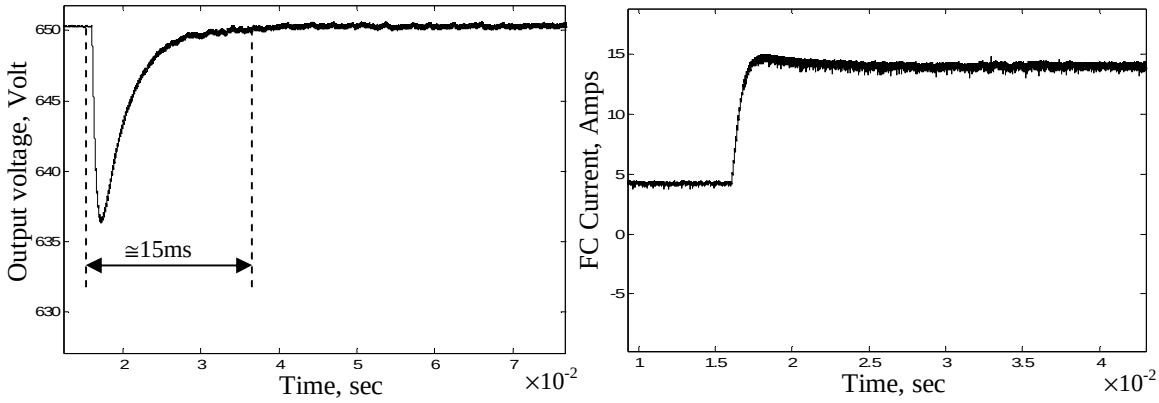
As stated in Section 4.3.2, with a suitable scaling for the digitized sensed output voltage and FC current, $K_{\_v}$ and $K_{\_i}$ can be set equal to 1. To do so, a fixed-point (fixdt(1,32,15)), shift arithmetic blocks, and IQN mathematical functions[9] blocks available in TI C2000 Toolbox in Simulink, have been used (see Appendix G, Fig. G.2).

The digital controllers for the current and voltage loop shown in Fig. 4.17 have been designed using a 32-bit digital PI compensator with anti-windup correction (see Appendix G, Fig. G.3). The output of the controller is connected to the PWM scaling in order to adjust the duty cycle as a per-unit between 0 and 1. A PWM generator has been developed that produces switching signals for the bridge switches as well as the clamp switch with only one modulating signal of 20 kHz (see Appendix G, Fig. G.4).

[8] Since the analogue input voltage range for the on-chip ADC converter of TMS320F2812 DSP is restricted between 0V to 3.0V, the SCU is required. If the input voltage to the on-chip ADC is outside range the multiplexer will be working in an unpredictable way giving incorrect values.

[9] IQN mathematical functions are provided by TI library to use the internal hardware of the DSP in the most efficient way. In effect, it virtualises the fixed-point processor as a floating-point system. IQN mathematical functions using IQ format (I: Integer, Q: Fraction) increase the precision but at the expense of the dynamic range.

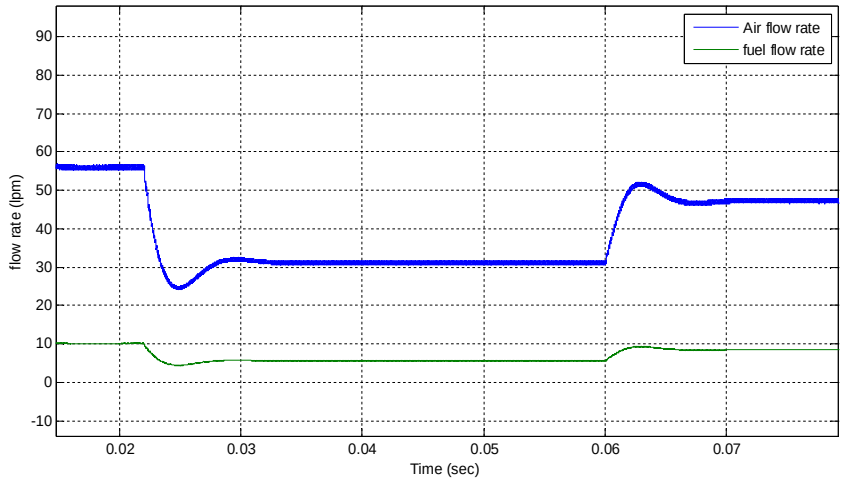
Fig. 4.18 shows that the system has a fast and stable response to a sudden load change and the ripple on FC current is very low.



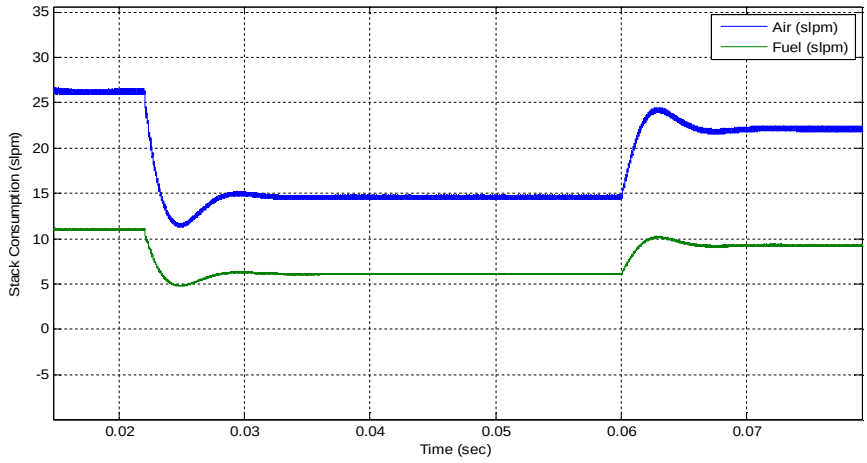
(a) (b)

Fig. 4.18 Converter dynamic response 500W to 205W: a) output voltage b) FC current

As described in Section 2.2, the system model includes a detailed PEMFC model, and Fig. 4.19 shows the stack consumption and flow rate of air and fuel under different FC load demands.



(a)



(b)

Fig. 4.19 SLPS simulation results of (a) stack consumption and (b) fuel and Air flow rate

It can be seen from Fig. 4.15 and Fig. 4.18, that the responses obtained from the small-signal model with closed-loop control closely resemble those of the full system based on the PCM approach, which inspires confidence in the validity of the approach in designing the closed-loop controllers.

The response of the output voltage following a step load change obtained through SLPS co-simulation confirms the ability of simulated converter to maintain the DC bus voltage within an acceptable tolerance and achieve a small current ripple in the output of the FC, which is beneficial for its longevity. However, Fig. 4.15 and Fig. 4.18 show there is a slight difference between the simulation results of the small-signal mathematical model approach and PCM approach. The main reason is that the simulation results of the PCM in PSpice uses accurate models of the power converter components including parasitic effects such as capacitances, stray inductances, and non-linear behaviour of the passive components and active switching devices. The latter would be difficult to incorporate in detail in the mathematical dynamic model of the power converter. Therefore, the benefit of PCM approach is that the modelled

performance of the converter will closely resemble that of an actual converter circuit and the efficiency can be estimated before the actual converter system is constructed.

It is worth mentioning here that the developed PSpice/Simulink integration via SLPS increases the fidelity of the plant modelling and enables the plant and the controller to be simulated in the same environment. In addition, the required simulation time is less than when the simulators are used individually (i.e. Simulink alone or PSpice alone).

4.6 Implementation and Validation of the Controller System

With the new dynamic model and the closed-loop controller designed, simulated, and verified, the validation of the control algorithm implementation can follow. To assess the control algorithm before applying it to the real converter, a new validation approach has been developed based on Processor-In-the-Loop (PIL) co-simulation. In this approach the source code is executed on the target DSP and then integrated with the model of the physical converter system running in Simulink, as will be described in Section 4.6.3.

After the functionality of the produced code has been evaluated, the developed control algorithm can be applied to the real converter and implemented using Model-Based Design approach (MBD), as will be shown in Section 4.6.4.

The following sections briefly describe details of the implementation of a digital PI controller on a F2812 DSP using the MBD approach.

4.6.1 MBD Approach Features

Model-Based Design means that one can simulate the controller of the power electronic system off-line using graphical blocks and signals. Once the controller design is verified, automatic code can be generated for the control subsystem and then run on the

embedded target in real time. MBD is one of the most efficient and cost-effective approaches to improve the reliability and quality of a system and reduce the required time for code development and validation.

A number of software packages are now available that can be employed to develop control systems rapidly by using a block-diagram programming model. Examples are the Real Time Workshop (RTW) with Embedded Target software from Mathworks, Embedded Controls Developer from VisSim and LabVIEW from National Instruments [112-115]. Matlab/Simulink with RTW is undoubtedly considered to be the best simulator environment and can be used for the MBD approach since it includes a large toolbox for signal processing and control system design. For the Texas Instruments C2000 family, such as TMS320F2812, Matlab provides a specific library of building blocks, such as on-chip ADC module, PWM module, GPIO module, and CAN module, that allows the user to drag-and-drop these blocks into the Simulink model and readily generate C-code. Also, the TI C2000 package provides two further special libraries equivalent to functions in the TI C28x assembly code library which are written to obtain very efficient code generation [116]. These libraries are IQmath and Digital Motor Control (DMC).

A number of MBD approaches have been proposed using Matlab and Simulink with RTW based on dSpace, microcontrollers or the F28x family processors [116-119]. From a cost point of view, the eZdsp F28x evaluation board developed by Digital Spectrum (see next section for further details about this board) has a lower price than the other environments such as the dSpace. Unfortunately, the Embedded Target software for TI C2000 DSPs has limited graphical programming features in comparison to dSpace because of the limited hardware interface resources in the eZdsp F28x board, with the

result that this board may not meet the requirements for all applications. These limitations can be reduced effectively by using additional features such as CAN, SCI, and SPI that are available with the eZdsp F28x board, but at the cost of requiring additional cables and transceiver cards. Nevertheless, Embedded Target software for TI C2000 DSP is a useful development tool to assist in rapid prototyping.

4.6.2 Selection of Embedded DSP

The F2812 DSP is a high performance 32-bit fixed-point DSP. This processor has specialised functions for use in control applications for electrical machines and power electronic circuits. To develop and run software for the F2812 processor and to permit full-speed verification of the code, Digital Spectrum has developed a stand-alone module called eZdspF2812 for the F2812, which includes 150 MIPS operating speed, 18Kb on-chip RAM, 128Kb on-chip Flash memory, 30 MHz clock, 2 expansion connectors (analogue, I/O), 16 ADC and PWM channels [120]. The nominated F2812 DSP is compatible with the TI C2000 Library, which allows C-Code to be produced automatically from the Simulink model.

4.6.3 Control Algorithm Validation

After the correctness of the developed dynamic analysis had been verified (see Section 4.5) and before implementing the control algorithm developed in Section 4.6.4, the algorithm has to be validated.

While the PCM approach is effective in providing a high fidelity in modelling of the physical components of the converter plant with the control system, it cannot exactly capture the dynamics of the actual control algorithm which is running on the real processor hardware. Therefore, in this section a new approach is presented that can

accurately test the developed digital controller algorithm executed on the DSP in conjunction with the detailed model of the physical converter depicted in Fig. 3.11. The new approach integrates the SLPS simulation platform with the PIL software provided by Matlab. This integration is referred to as SLPS-PIL dual co-simulation. The term "dual co-simulation" reflects the division of work in which the physical converter model is running in PSpice and is integrated with the Simulink environment, which is simulating the FC power source model, load model, and DSP on-chip peripheral models, while the digital controller algorithm code runs on the actual processor hardware.

The SLPS-PIL dual co-simulation provides a test method to validate the controller source code on the actual processor hardware which controls a virtual prototype of a converter system that runs in PSpice. In order to explain the developed approach, Fig. 4.20 shows the basic architecture of the proposed SLPS-PIL dual co-simulation. It can be seen that SLPS-PIL architecture consists of two parts; hardware and software. The hardware parts involve the PC host, the eZdsp F28x evaluation board, the PCI bus, and the serial cable. The software parts are the OrCad/PSpice simulator, Matlab/Simulink simulator, code composer studio software (CCS3.3), TI C2000 toolbox package, Embedded IDE Link software, and the RTW.

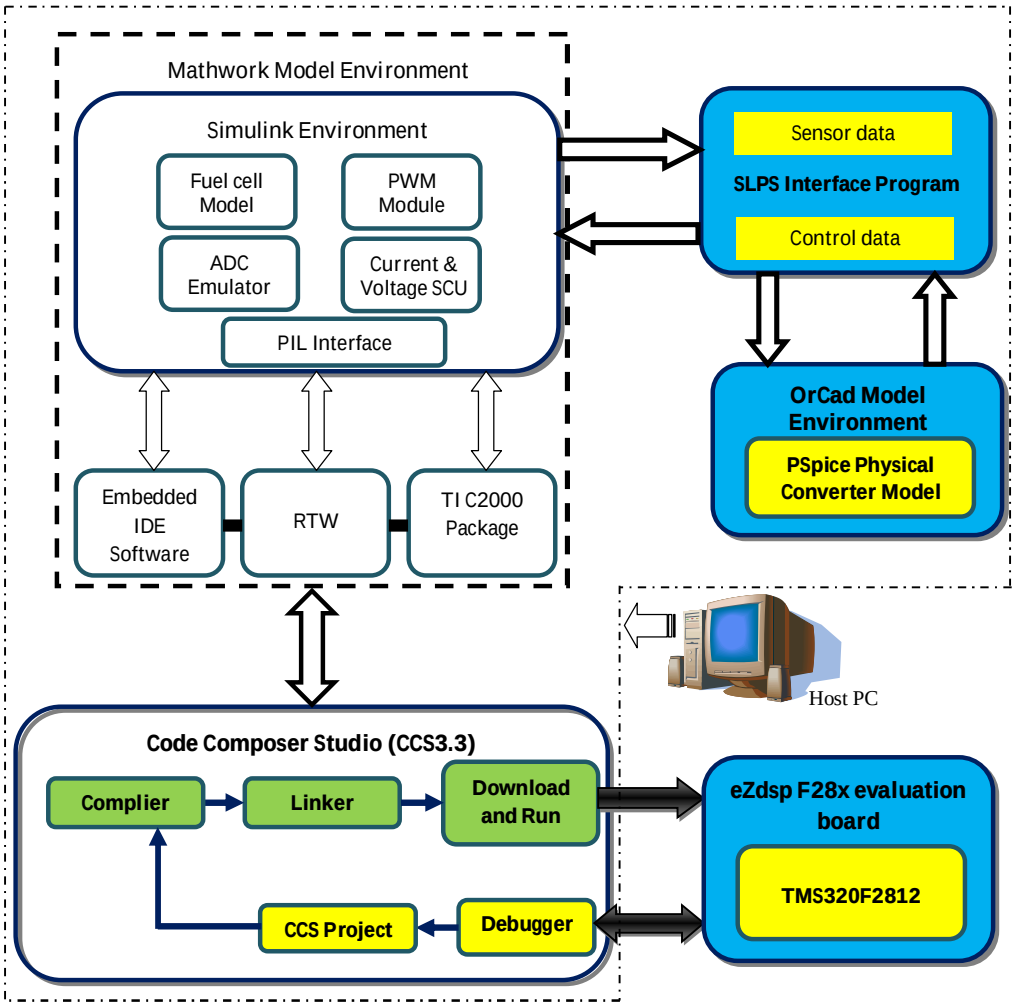


Fig. 4.20 Proposed SLPS-PIL integration architecture

As indicated in Fig. 4.20, during the SLPS-PIL dual co-simulation process, PSpice simulates the physical converter model and exports sensor and measurement output data, such as the output voltage and FC current, to the Simulink environment through SLPS. The data received by Simulink is exported to the digital controller algorithm that is executed on the DSP target. In this data exchange process, RTW generates an executable application for the PIL so that the controller code runs on the processor hardware for one sample interval. Then the processor is halted and is debugged the algorithm code using CCS3.3. Subsequently, the processed control signals enter Simulink via the PIL and RTW.

When Simulink receives the control signals from the processor, it updates the duty cycle in the PWM module and then exports the PWM, FC voltage, and the load signals to the model of the physical converter in PSpice via SLPS. At this instant, one sample cycle for the SLSP-PIL dual co-simulation is completed and the converter plant in PSpice proceeds to the next sample interval. The SLPS-PIL dual co-simulation exchanges data with the DSP through the PCI bus and the serial port cable.

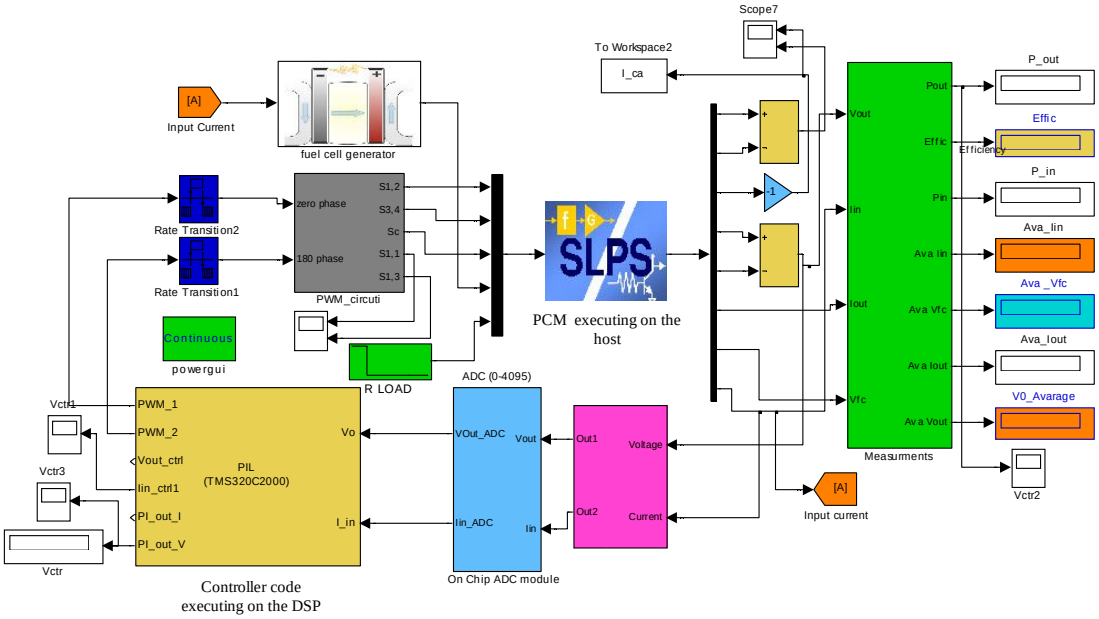


Fig. 4.21 Simulink schematic diagram of the proposed SLPS-PIL dual co-simulation

Fig. 4.21 shows the simulation model of the developed SLPS-PIL dual co-simulation method, where the PIL block is replaced by the controller subsystems of Fig. 4.17. In this approach, C-code is generated for the controller algorithm and then cross-compiled and downloaded onto the actual embedded target using Embedded IDE Link software with RTW in Matlab.

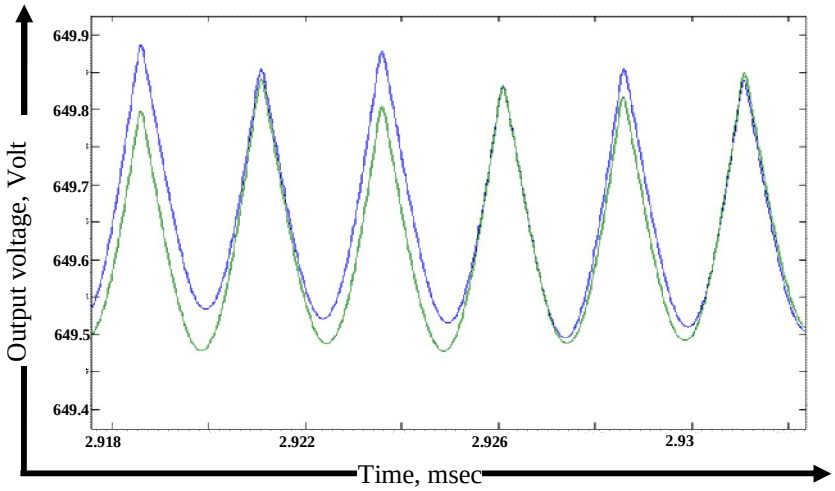


Fig. 4.22 PCM approach results (blue) against SLPS-PIL dual co-simulation results (green)

As shown in Fig. 4.22 , SLPS-PIL dual co-simulation results show an excellent match with the PCM approach results of Section 4.5.2, which confirms the validity of the generated developed controller code algorithm. However, as shown in Fig. 4.22, a small error is noticed less than 0.1V between the PCM approach results and SLPS-PIL dual co-simulation results. This error can be reduced further by using Vector Scope instead of common Scope from Simulink library.

For the next, the emulated ADC and PWM blocks in Fig. 4.17 will be replaced with hardware blocks that consist of the ADC module, the PWM module and the Hardware Interrupt block (see Fig. 4.24). This stage can therefore be described as a period in which the project transfers from simulated time to real time.

4.6.4 Control Algorithm: Testing and Performance

Once the converter's efficiency had been measured and compared with other topologies using the open-loop test (see Appendix H), the digital average current-mode controller algorithm was deployed on the DSP as described below.

Even with careful layout design (see Section 3.3), switching noise in the practical system, caused by the turning on or off of the power electronic devices, is inevitable. The switching noise in the measured inductor current or output voltage can cause inaccuracy in the readings of the ADC converter and may distort it. Analogue filtering, such as low pass filtering (LPF) of this high frequency noise could be used for cleaning-up of the measured signals but it would cause a destabilising delay in the feedback loop and reduce the bandwidth of the designed digital controller.

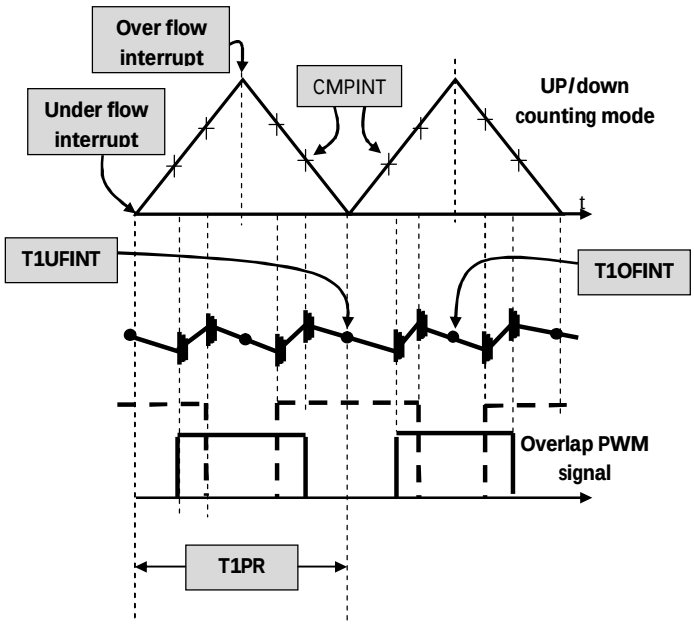


Fig. 4.23 Sampling Interrupts for the measured signals

With the Event Manager Module in the F2812 it is possible to generate up to four interrupts: timer underflow interrupt (TxUFINT), period interrupt (TxPINT), Compare Match Interrupt (CMPxINT), and Timer overflow interrupt (TxOFINT). As can be seen in Fig. 4.23, the measurements are triggered by the under and overflow interrupts to overcome the impact of noise without the need for a large LPF at the input of the on-chip ADC peripheral. This method effectively filters the measured signal by taking the average of it digitally.

To test this strategy it was implemented using Embedded IDE Link with RTW, as shown in Fig. 4.24. Initially to provide access from Simulink to the processor hardware, a F2812eZdsp stand-alone block was selected to set the processor preferences for the model. The triggered subsystem block implements the current-controller for the converter so that the controller is interrupt-driven by the hardware interrupt block.

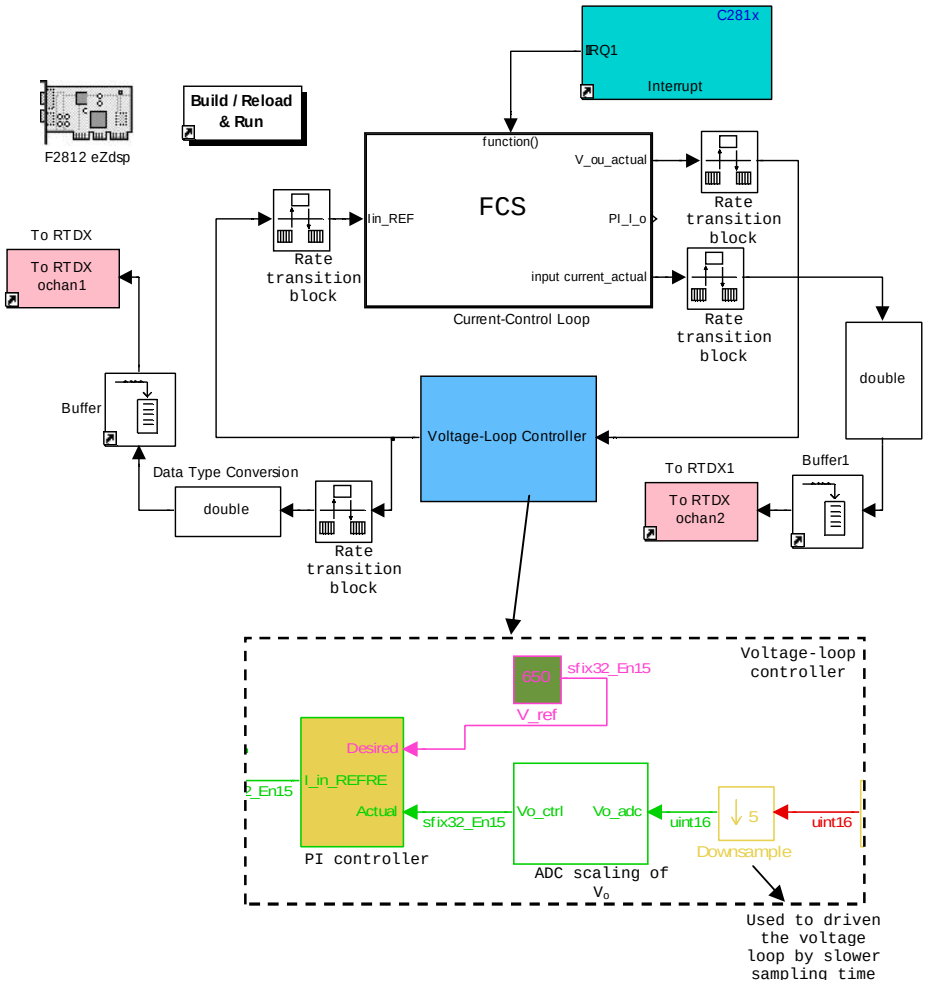


Fig. 4.24 MBD implementation block diagram of the two-loop digital controller

The Interrupt Service routine (ISR) provided by the Hardware C28x interrupt block (with PIE interrupt = 6 and CPU interrupt = 1) is connected to the Function Call Subsystem (FCS) to enable the Event Manager A (EVA) to generate a Start-Of-Conversion (SOC) command for the ADC so that the current-loop respond faster than voltage-loop (blue block), as shown in Fig. 4.25.

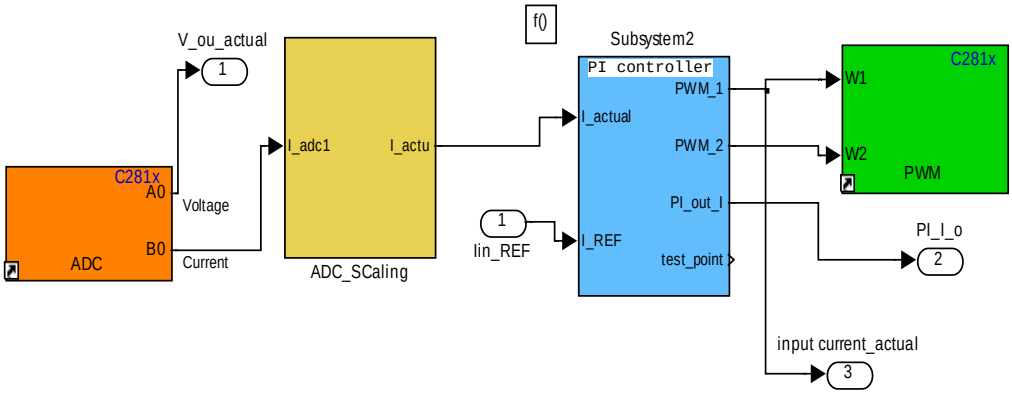
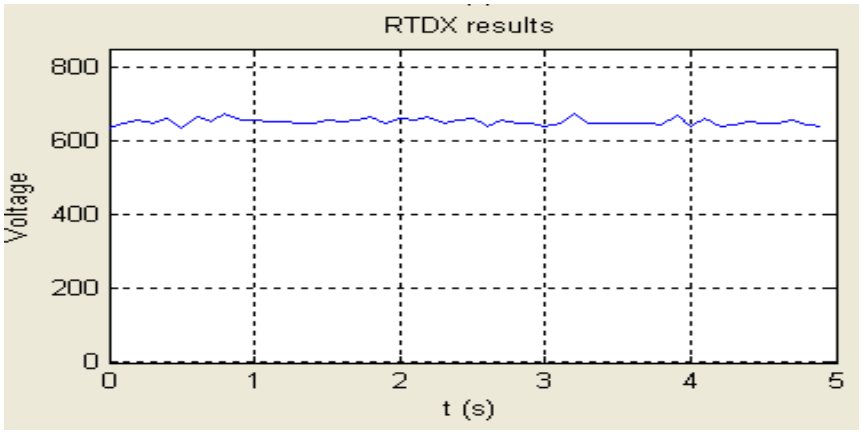


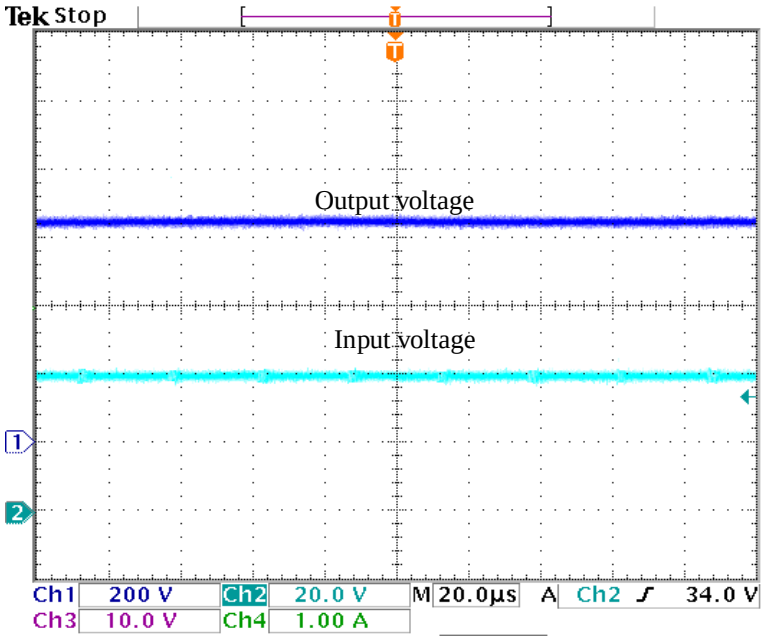
Fig. 4.25 Block diagram showing the blocks inside the current-control loop in Fig. 4.24

Inside the FCS, the ADC is trigger at the period time, which is set in the PWM block module, and an interrupt is posted at the end of the ADC conversion, which is set using ADC block module. Hence, the ISR is called at every time period and it is used to update the duty cycle at the start of the subsequent PWM cycle. The ADC signal output is software scaled, so that the digitized output value of the acquisition stage resembles the units of the measured physical signals. These scaled signals are then used for the voltage and current controller subsystems.

As shown in Fig. 4.24, the sample time of the outer voltage loop is slowed down by the “Down-Sample” block since this outer loop should be slower than the inner current loop. Several “Rate Transition” blocks are used because the utilized blocks are running at different sample times. The sample time of the FCS is set to (-1) since this block is triggered by ISR every 50µs.



(a)



(b)

Fig. 4.26 Output voltage of the FC converter measured by using (a) RTDX and (b) the oscilloscope

Fig. 4.26 shows how the output voltage is regulated using the proposed algorithm, where Fig. 4.26a show the output voltage waveform measured via RTDX and plotted using the developed GUI display, while Fig. 4.26b show the output and input voltage

waveforms measured by the Oscilloscope. A well matching between the two figures can be observed.

4.7 Conclusion

In this Chapter, a dynamic model based on state-space averaged method has been developed for the proposed FBCFC. A small-signal AC equivalent circuit of the converter is derived together with the significant small-signal transfer functions. In this Chapter, it has been demonstrated that the proposed converter not only has a higher efficiency (as shown in Chapter 3) but also exhibits a more favourable dynamic behaviour than other competing CFC topologies. The dynamic model presented in this work is utilized to systematically design a digital average current-mode controller for the FC power converter system. Different approaches have been presented in order to verify the developed dynamical model and to evaluate the performance of the converter controller. The results have demonstrated the consistency of the developed dynamic model and the effectiveness of the digital controller. They have shown that the proposed SLPS-PIL dual co-simulation provides an optimum method for bridging the gap between the simulation model and the final FC converter system implementation. In addition, it is shown that the SLPS-PIL dual co-simulation not only increases the fidelity of the converter model but also represents the exact digital controller dynamics.

Besides, in this Chapter, a method of code generation for a two-loop digital PI controller for the converter using the Model Based Design approach has been developed. Model Based Design implementation has resulted in efficient code generation for the controller design that reduces the code generation time, optimises the generated C-Code and speeds up the algorithm execution.

Chapter Five

Controlling Power Flow Methods for the Bidirectional Converter: A Comparative Study

5.1 Introduction

As described in Chapter 2, for interfacing an ultracapacitor (UC) to the DC link of a DC microgrid a bidirectional DC-DC converter (BDC) is needed. Hence, the BDC manages the power flow between the FC generator, UC storage, and the load. As shown in Section 2.5, both voltage-fed and current-fed topologies can be used as a BDC. Because the latter has a non-minimum-phase characteristic, the voltage-fed BDC is better suited for dealing with the fast transient power changes due to variable loads. The voltage-fed BDC has a number of attractive features such as zero-voltage switching (ZVS), lower number of passive components, and low voltage ratings compared to the current–fed BDC configuration.

By combining the voltage-fed BDC with a voltage-doubler circuit, as shown in Fig. 5.1, a converter with a lower number of active devices at the lowest voltage rating and further efficiency improvement can be realised. Therefore, this topology has been used for further investigation.

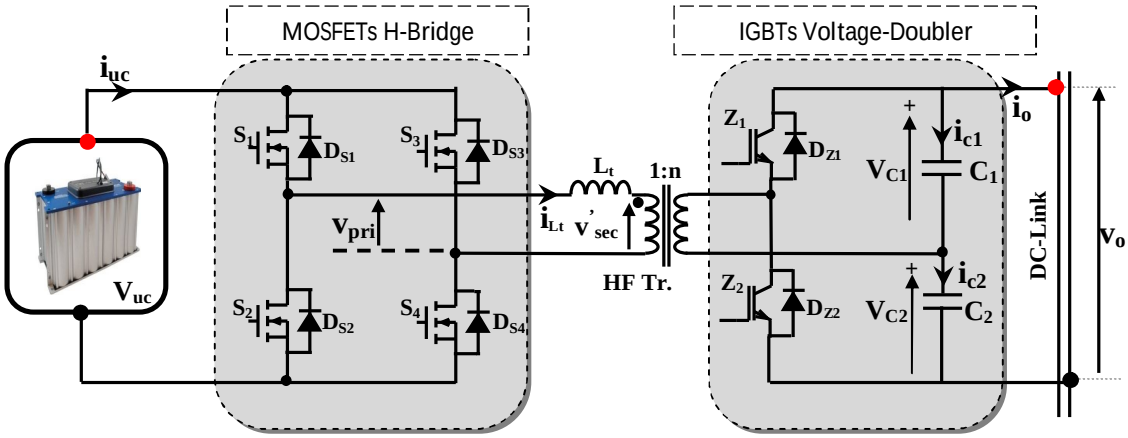


Fig. 5.1 Schematic of the BDC with voltage-doubler on high-voltage side

Typically BDCs use a phase-shift control strategy (presented in the next Section) to control the transfer of power in both directions. However, the BDC operation with a phase-shift control cannot maintain soft-switching (SSW) for a wide UC voltage variation[1] and exhibits a higher circulating power flow, a higher RMS current and higher conduction losses as a consequence. Therefore, alternative modulation methods for the BDC are necessary.

In this Chapter, an overview of several modulation methods that have been proposed in the literature to control the power flow of the BDC for the UC application are presented.

5.2 Conventional Phase-Shift Modulation Scheme

According to Chapter 2, the BDC uses the phase-shift φ between the voltages across both sides of the isolation transformer to control the transfer of power through the series inductance L_t in both directions[2]. This type of modulation is called here conventional phase-shift control (CPC) modulation [84, 121] (also named as "Rectangular Modulation" [122-124]).

[1] The output voltage of the UC energy buffer varies widely compared to the batteries, typically between 24V to 48V for the Maxwell Boostcap™ ultracapacitor Model BMOD0165 (165F, 48V).
[2] The series inductance L_t is the transformer leakage inductance plus a possible external inductance (see Section 6.2.2).

The power flow directions of the BDC are defined as:

- Ultracapacitor charging mode (UCCM): where the average power P_{uc} transfers from DC link side to UC side and $P_{uc} < 0$, $\varphi < 0$
- Ultracapacitor discharging mode (UCDM): where the average power P_{uc} transfers from UC side to DC link side and $P_{uc} > 0$, $\varphi > 0$

If the output voltage V_o assumed constant[3], the primary voltage $v_{pri}(t)$, the secondary voltage referred to the primary $v'_{sec}(t)$, the voltage across the series inductance $v_{Lt}(t)$, and the primary current $i_{Lt}(\theta)$ waveforms can be plotted as shown in Fig. 5.2 for different UC voltage. This figure assumes that the BDC is operating under CPC and transfers power from the UC to the DC link (i.e. UCDM).

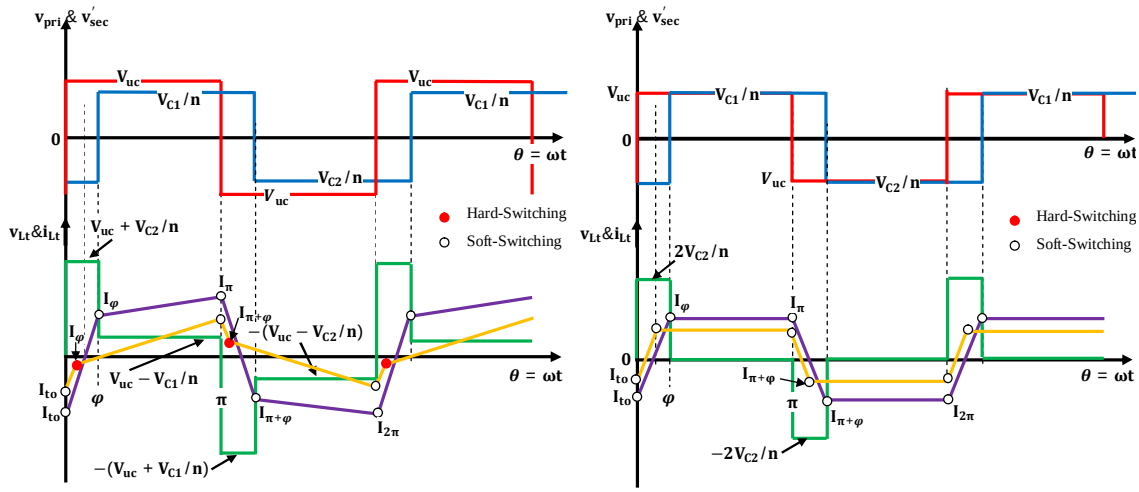
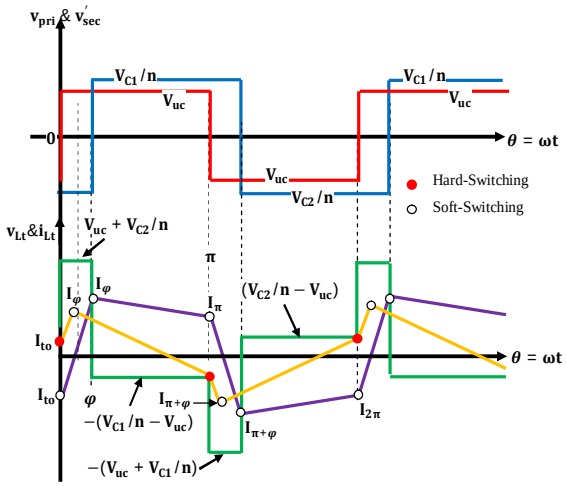


Fig. 5.2 Voltage and current waveforms of the BDC operating under CPC modulation for the different UC voltage and under UCDM (continued on the next page)

[3] This assumption based on that the output of the BDC is connecting to the regulated DC link.



(c)

Fig. 5.2cont. Voltage and current waveforms of the BDC operating under CPC modulation for the different UC voltage and under UCDM: (a) $2nV_{uc} > V_o$, (b) $2nV_{uc} = V_o$, and (c) $2nV_{uc} < V_o$ (Note: yellow and purple waveforms are the primary current plotted for the same V_{uc} and V_o but at the different phase-shift angle φ)

As can be seen in Fig. 5.2a-c, when using CPC all BDC switches are driven at 50% duty cycle and the transferred power is controlled by the phase-shift φ only. Hence, the primary voltage $v_{pri}(t)$ is either $+V_{uc}$ or $-V_{uc}$ and the secondary voltage referred to the primary $v'_{sec}(t)$ is either $+V_o/2n$ or $-V_o/2n$[4]. It is obvious that the waveform shape of the primary current[5] $i_{Lt}(\theta)$ determines by the voltage difference across the series inductance (L_t). This voltage difference is determined by the amplitude of the primary voltage V_{uc} and the amplitude of the secondary voltage referred to the primary $V_o/2n$.

As can be seen in Fig. 5.2a-c the waveform of the primary current $i_{Lt}(\theta)$ is symmetrical, hence, only the first half-cycle (time interval T_1: $0 < \theta < \varphi$ and time interval T_2: $\varphi < \theta < \pi$) needs to be considered. Based on that, Table 5.1 lists the equations for the primary current $i_{Lt}(\theta)$ during the first half-cycle for different V_{uc} and for both BDC modes (UCCM and UCDM).

[4] Notice the principle of operation here is based on the selected BDC shown in Fig. 5.1.
[5] The primary current is the same as the current through the series inductance L_t.

TABLE 5.1
EXPRESSION OF THE PRIMARY CURRENT $i_{LT}(\theta)$ FOR THE DIFFERENT UC VOLTAGE AND FOR BOTH BDC MODES (UCCM AND UCDM)

		$2nV_{uc} > V_o$	$2nV_{uc} = V_o$	$2nV_{uc} < V_o$
UCDM	T_1	$i_{Lt}(\theta) = \left(\frac{\frac{V_{C2}}{n}+V_{uc}}{\omega L_t}\theta\right) + i_{Lt}(0)$	$i_{Lt}(\theta) = \left(\frac{2V_{C2}}{n\omega L_t}\theta\right) + i_{Lt}(0)$	$i_{Lt}(\theta) = \left(\frac{\frac{V_{C2}}{n}+V_{uc}}{\omega L_t}\theta\right) + i_{Lt}(0)$
	T_2	$i_{Lt}(\theta) = \left(\frac{V_{uc}-\frac{V_{C1}}{n}}{\omega L_t}(\theta - \varphi)\right) + iLt\varphi$	$i_{Lt}(\theta) = i_{Lt}(\varphi) = i_{Lt}(\pi)$	$i_{Lt}(\theta) = \left(-\frac{\frac{V_{C1}}{n}-V_{uc}}{\omega L_t}(\theta - \varphi)\right) + iLt\varphi$
UCCM	T_1	$i_{Lt}(\theta) = -\left(\frac{\frac{V_{C1}}{n}+V_{uc}}{\omega L_t}\theta\right) - i_{Lt}(0)$	$i_{Lt}(\theta) = -\left(\frac{2V_{C2}}{n\omega L_t}\theta\right) - i_{Lt}(0)$	$i_{Lt}(\theta) = -\left(\frac{\frac{V_{C1}}{n}+V_{uc}}{\omega L_t}\theta\right) - i_{Lt}(0)$
	T_2	$i_{Lt}(\theta) = -\left(\frac{V_{uc}-\frac{V_{C1}}{n}}{\omega L_t}(\theta - \varphi)\right) - iLt\varphi$	$i_{Lt}(\theta) = -i_{Lt}(\varphi) = -i_{Lt}(\pi)$	$i_{Lt}(\theta) = -\left(-\frac{\frac{V_{C1}}{n}-V_{uc}}{\omega L_t}(\theta - \varphi)\right) - i_{Lt}(\varphi)$

It can be seen in Table 5.1 that the UCCM is the mirror image of the UCDM; therefore only the latter mode is considered for the following current and output power calculations. The average power P_{uc} that can be transferred during the UCDM can be given as

$$P_{uc} = \frac{2}{2\pi}\int_0^{\pi} v_{pri}(\theta).\, i_{Lt}(\theta)d\theta = \frac{V_{uc}}{\pi}\int_0^{\pi} i_{Lt}(\theta)d\theta \qquad (5.1)$$

Thus, to compute the transferred power P_{uc} the current $i_{Lt}(\theta)$ is required. Using the triangular and trapezoidal area calculation methods, the transferred power P_{uc} during the UCDM when $2nV_{uc} > V_o$ can be found as

$$P_{uc} = \frac{V_{uc}}{2\pi}\left((I_{to} + I_{\varphi})\varphi + (I_{\varphi} + I_{\pi})(\pi - \varphi)\right) \qquad (5.2)$$

The values of the currents I_{to}, I_{φ}, and I_{π} at the commutation instants 0, φ, and π can be obtained as[6]:

$$I_{to} = -\frac{(-\pi + \varphi)V_{C1} + \varphi V_{C2} + n\pi V_{uc}}{2n\omega L_t} \tag{5.3}$$

$$I_{\varphi} = \frac{(\pi - \varphi)V_{C1} + \varphi V_{C2} - n(\pi - 2\varphi)V_{uc}}{2n\omega L_t} \tag{5.4}$$

and

$$I_{\pi} = -I_{to} = \frac{(-\pi + \varphi)V_{C1} + \varphi V_{C2} + n\pi V_{uc}}{2n\omega L_t} \tag{5.5}$$

Using (5.2)-to-(5.5), the transferred average power P_{uc} of the BDC under CPC for the UCDM operation and for $V_{C1}=V_{C2}=V_o/2$ can be given as:

$$P_{uc} = \frac{V_o V_{uc}}{2n\pi\omega L_t}(\pi - \varphi)\varphi \tag{5.6}$$

By equating the derivative of (5.6) to zero the maximum phase-shift angle $\varphi_{\max}^{CPC}$ is found equal to $\pi/2$. Hence, the maximum power $P_{uc\_max}^{CPC}$ that can be delivered by the BDC under CPC is:

$$P_{uc\_CPC}^{max} = \frac{\pi V_o V_{uc}}{8n\omega L_t} \tag{5.7}$$

Fig. 5.3 shows the achievable power transfer for the BDC under CPC when the UC voltage is changing between 100% to 50% of its rated voltage (see Section 2.3). It can be seen that BDC under CPC has the ability to deliver power beyond $\varphi_{\max}^{CPC}$ but at the expense of high circulating current through the switches, and higher conduction losses

[6]Using a similar procedure, I_{to}, I_{φ}, and I_{π} for $2nV_{uc}<V_o$ or $2nV_{uc}=V_o$ can be obtained.

as a consequence. At the phase-shift $\varphi = 180^0$ the power delivered by the BDC under CPC is 0W. It should be noted that in practice the converter is not able to deliver 0W due to the effect of the fall and rise time of the gate signals [125]. As can be seen in (5.7), the maximum achievable power P_{uc}^{max} is not only limited by the maximum phase-shift angle but also by the series inductance L_t and the transformer turns ratio n. Hence, L_t and n must be selected based on the required rated power for the BDC with respect to the lower RMS current (see Sections 5.2.2 and 6.2.2).

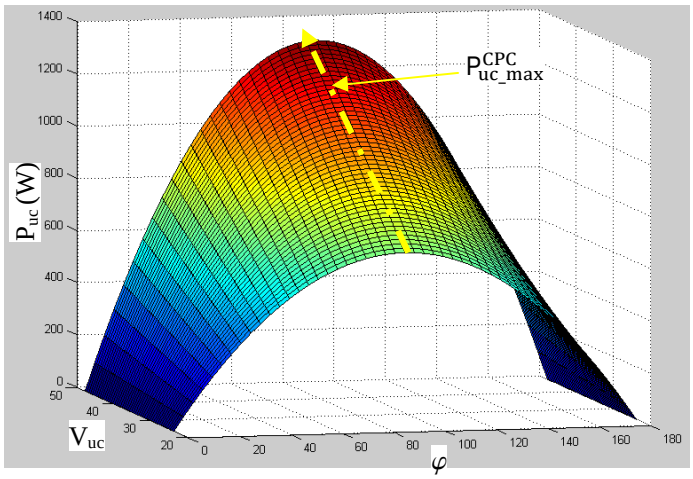


Fig. 5.3 3D contour surfaces of the BDC power flow under CPC modulation (L_t=10 µH, n=7.4, V_o=650V, and f_s=20kHz)

5.2.1 SSW Analysis

From (5.6), it is evident that the power of the BDC under CPC can be controlled by varying φ only and for that reason the CPC modulation method has been used widely [84, 121, 126], because of its simplicity of implementation. In addition, the BDC under CPC has the highest power transfer capability of any modulation scheme [127]. Also, one of the CPC advantage is that the switching devices at both BDC sides are capable of operating with zero-voltage switching (ZVS) for the entire phase-shift angle range (Fig. 5.2b)[128]. However, this is only possible when the following conditions are valid:

$$I_{to} < 0,\ I_{\varphi} > 0,\ I_{\pi} > 0, \text{ and } I_{\pi+\varphi} < 0 \tag{5.8}$$

The above SSW conditions mean that the values of the currents (I_{to}, I_{ϕ}, I_{π}, and $I_{\pi+\varphi}$) at the switching instants 0, φ, π, and $\pi+\varphi$ must be sufficient to discharge and charge the parasitic capacitances of the switches (S_1~S_2, Z_1, S_3~S_4, and Z_2) during the dead periods in order to ensure zero-volts before the switches are conducting (see purple and yellow waveforms in Fig. 5.2 a-c). Fig. 5.4 details what the required amount of these currents I_{to}, I_{ϕ}, and I_{π} and $I_{\pi+\varphi}$ is to ensure ZVS for the BDC switches S_1~S_2, Z_1, S_3~S_4, and Z_2 respectively. Notice that Fig. 5.4 a-d is plotted for the wide variation in the UC voltage with an entire power range[7].

[7] The available power range is proportional to the entire allowable phase-shift φ in the CPC, as shown in Fig. 5.3.

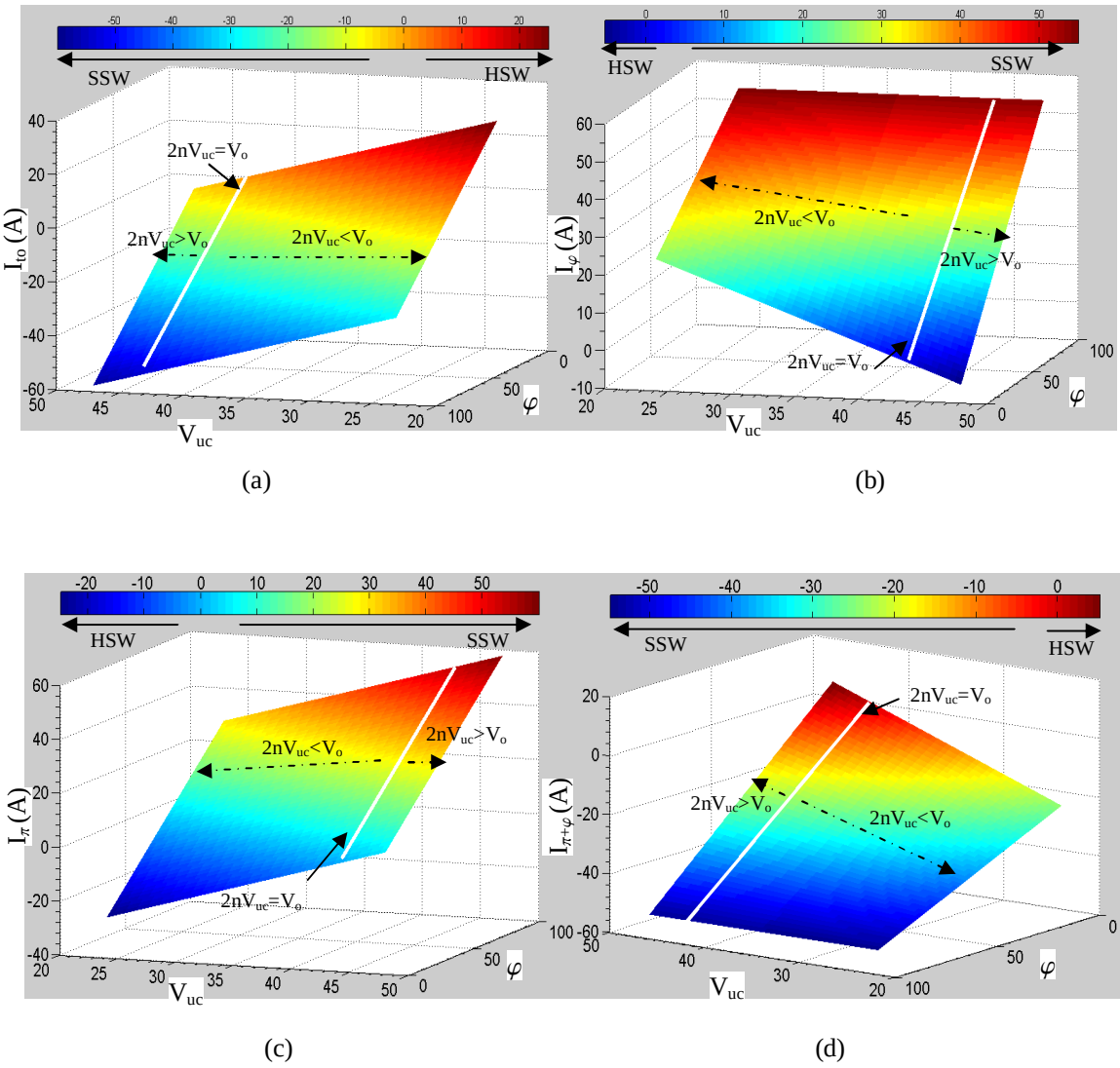


Fig. 5.4 3D contour surface shows the available current via the series inductance L_t at the commutation instants 0, φ, π, and $\pi+\varphi$: (a) I_{to}, (b) I_{φ}, (c) I_{π} and (d) $I_{\pi+\varphi}$

From Fig. 5.4a it can be seen, that the value of the current I_{to}, when the UC voltage is low (i.e. $2nV_{uc}<V_o$), is not sufficient to discharge the parasitic capacitances of the diagonal switches S_1~S_2 at the medium and light loads. Thus, S_1~S_2 are operating under HSW for this load and UC voltage range. In contrast, when the UC voltage increasing (i.e. $2nV_{uc} > V_o$) the value of the current I_{φ} is not sufficient to discharge the parasitic capacitances of the switch Z_1, resulting in a failure to realize ZVS for Z_1 under the light load, as indicated in Fig. 5.4b. Similar to Fig. 5.4a, Fig. 5.4c shows that ZVS is not realised for the other diagonal switches S_3~S_4 at the switching instant π when $2nV_{uc}<V_o$

due to the small value of the current I_π. The ZVS for the voltage-doubler switch Z_2 fails at the turn-on instant $\pi+\varphi$ when $2nV_{uc}>V_o$, as shown in Fig. 5.4d. This is due to insufficient energy available from the series inductance L_t (i.e. $I_{\pi+\varphi} > 0$) to discharge the parasitic capacitance of Z_2.

However, it can be noted that SSW operation is only possible when the amplitude of the secondary voltage reflected to the primary $v'_{sec}(t)$ is equal to the amplitude of the UC voltage V_{uc} (i.e. $2nV_{uc}=V_o$, see the white lines in Fig. 5.4a-d) and both voltages remain essentially constant (e.g. fixed-voltage DC-DC converters or battery chargers/dischargers). Thus, the BDC operating under CPC has a limited soft-switching range when operated with sources that have a wide input voltage variation, such as UCs.

Another disadvantage of the CPC method is that it increases the RMS current and the conduction loss in the BDC parts. This is can be clarified as described next.

5.2.2 RMS Analysis

The RMS primary current I_{rms} through the BDC when it is operating under CPC in UCDM can be given as:

$$I_{rms} = \sqrt{\frac{1}{2\pi}\left[\int_0^{2\pi} i_{Lt}^2(\theta)\,d\theta\right]} \tag{5.9}$$

Using equations in Table 5.1, (5.3), (5.4), and (5.5), the RMS current when $2nV_{uc} = V_o$ and $2nV_{uc} > V_o$ respectively are given as:

$$I_{rms} = \frac{\sqrt{3\pi - 2\varphi}}{\sqrt{3\pi}}\frac{V_o}{2n\omega L_t}\varphi \tag{5.10}$$

and

$$I_{rms} = V_o \frac{\sqrt{(7\pi^3 - 24\pi^2\varphi + 30\pi\varphi^2 - 12\varphi^3)}}{4n\sqrt{3\pi}\omega L_t} + \frac{\sqrt{n(-7\pi^3 + 18\pi^2\varphi - 12\pi\varphi^2 + 2\varphi^3)V_o V_{uc}}}{2n\sqrt{3\pi}\omega L_t} + V_{uc}\frac{\sqrt{\pi(7\pi^2 - 12\pi\varphi + 6\varphi^2)}}{2\sqrt{3\pi}\omega L_t} \quad (5.11)$$

From (5.6) , the required series inductance L_t can be obtained as:

$$L_t = \frac{V_o V_{uc}}{2n\pi P_{uc}\omega}(\pi - \varphi)\varphi \quad (5.12)$$

Substitute (5.12) in (5.10) and (5.11), the relation between the RMS current I_{rms}, the transferred power P_{uc}, and the phase-shift φ is given as

$$I_{rms} = \frac{\pi\sqrt{1 - \frac{2\varphi}{3\pi}}}{(\pi - \varphi)V_{uc}} P_{uc} \quad (5.13)$$

and

$$I_{rms} = \sqrt{\frac{\pi}{3}}\frac{P_{uc}}{2(\pi - \varphi)\varphi V_o V_{uc}}\left(V_o\sqrt{(7\pi^3 - 24\pi^2\varphi + 30\pi\varphi^2 - 12\varphi^3)} + 2\sqrt{nV_o V_{uc}(-7\pi^3 + 18\pi^2\varphi - 12\pi\varphi^2 + 2\varphi^3)} + 2nV_{uc}\sqrt{\pi(7\pi^2 - 12\pi\varphi + 6\varphi^2)}\right) \quad (5.14)$$

for $2nV_{uc} = V_o$ and $2nV_{uc} > V_o$ respectively.

The relationships (5.13) and (5.14) between the primary RMS current and the phase-shift φ for the two cases at the same power are shown in Fig. 5.5.

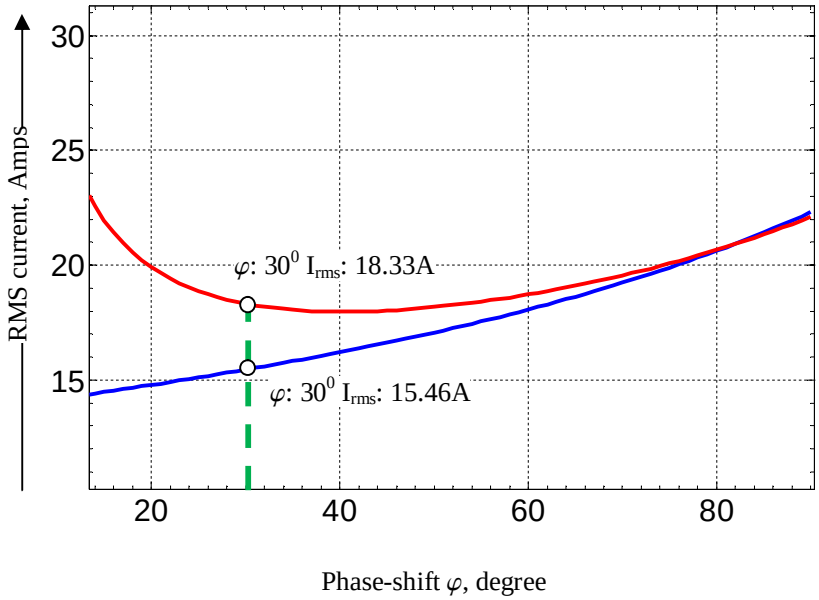


Fig. 5.5 Primary RMS current when $2nV_{uc} > V_o$ (red) and $2nV_{uc} = V_o$ (blue) (P_{uc} = 600W, V_o = 650V, n = 7.4, and f_s =20kHz)

It is clear that the RMS current of the BDC under CPC increases at higher φ values and that the BDC has a higher RMS current when the UC voltage increases (i.e. $2nV_{uc} > V_o$). Thus, from the view of higher efficiency it is desirable for the BDC under CPC to operate: ① with a smallest phase-shift φ and ② when $2nV_{uc} = V_o$. However, this is at the detriment of the power transfer capability of BDC and its use in UC applications.

The disadvantage of CPC modulation have led many authors to find alternative modulation approaches, seeking to extend the SSW range and improve the performance and the efficiency of the BDC. Some of those approaches are described in the next section.

5.3 Alternative Phase-Shift Modulation Schemes

In the present application, the BDC is needed to connect the UC with the DC link of the DC microgrid. Based on the specifications of the Maxwell Boostcap^{TM} ultracapacitor Model BMOD0165 described in Section 2.3, the operating voltage range of this model is between 48V to 24V. Thus, the input voltage of the BDC varies significantly. Hence,

as clarified in the previous section, due to the high switching and conduction losses the CPC is not the preferable modulation for the BDC circuit when it is operating with a source with a wide input/output voltage. Therefore, to minimise the losses and improve the BDC performance an alternative modulation is required.

Many topologies have been proposed to minimise the conduction loss and extend the SSW range for the BDC. These topologies can be divided into two main approaches: the first approach is based on using additional components with the BDC such as use a resonant circuit, a variable AC link reactance, and a snubber circuit [91, 129-135]. While this approach extends the soft-switching for the converter's switches, the result is an increase of the circulating currents, with a higher conduction loss as a consequence, as well as higher converter costs[8]. The second approach is to modify the switching control strategy of the CPC modulation without adding any additional components. This approach is called here alternative phase-shift modulation (APM). The APM uses the phase-shift between the primary and secondary voltages to deliver the required power while changing the duty cycle of the converter bridges to maximise operating efficiency of the BDC. However, improving the efficiency using this approach is on account of increasing the complexity of implementing the switching controller. Nevertheless, this approach is very smart and therefore has attracted many authors [19, 122, 130, 136-143] since it minimises the losses without adding more passive or active components. Some of the APM schemes are described below.

5.3.1 Triangular Current Modulation

In [127, 137, 142], an APM scheme called triangular current modulation (TRM) is proposed to reduce the circulating current through the converter by shaping the current in the primary winding to a triangular waveform, where the two BDC bridges shown in

[8] Some types of those converters were discussed in Chapter 2.

Fig. 5.6 are driven with a variable duty cycle. The key waveforms of this modulation scheme are shown in Fig. 5.7.

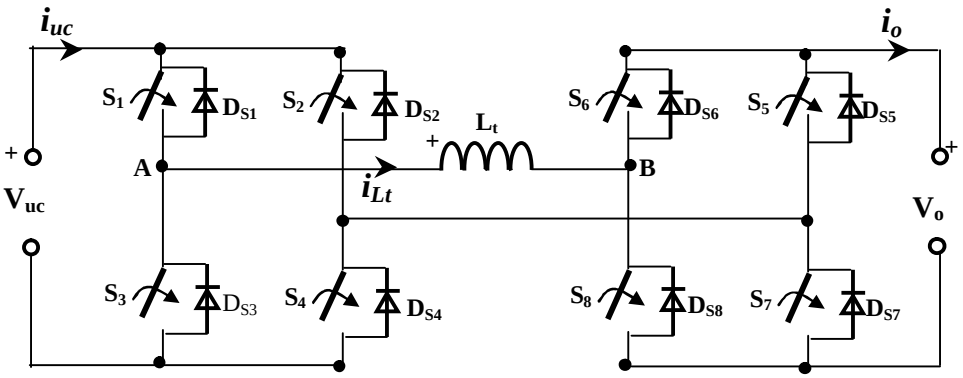


Fig. 5.6 Schematic Diagram of the BDC with two H-bridges

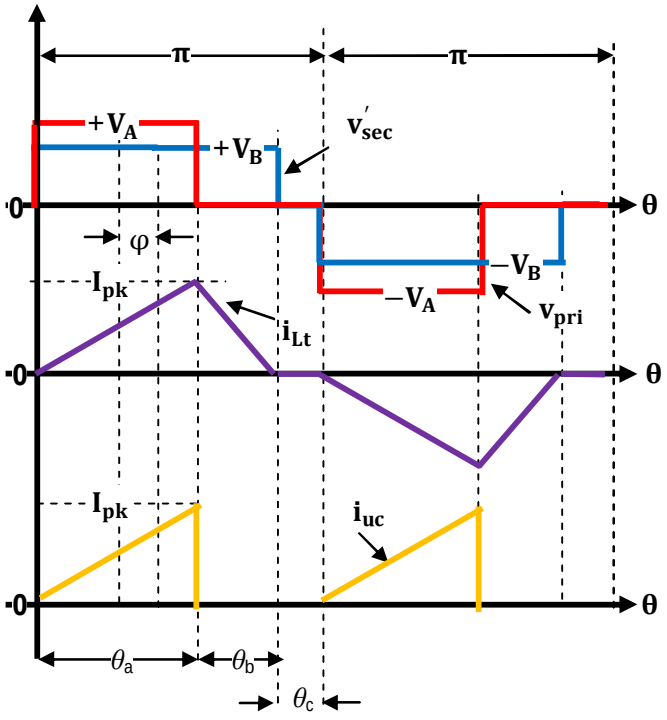


Fig. 5.7 Key waveforms of the TRM scheme , when $V_A > V_B$ and the BDC under UCDM

As shown in Fig. 5.7, the operational modes of the BDC under TRM and $V_A > V_B$ can be divided into 6 modes over one cycle. The two half cycles are complementary. Unlike CPC, the states of the primary voltage $v_{pri}(t)$ over one cycle fluctuates as ($+V_A$, 0, 0, -

V_A, 0, 0) and the state of the secondary voltage $v'_{sec}(t)$ fluctuates as ($+V_B$, $+V_B$, 0, $-V_B$, $-V_B$, 0,), where the voltages V_A ($V_A = V_{uc}$) and V_B ($V_B = V_o/n$) are the amplitude of the $v_{pri}(t)$ and $v'_{sec}(t)$ respectively. Hence, the primary current i_{Lt} during the periods θ_a, θ_b, and θ_c can be given as

$$i_{Lt}(\theta) = \begin{cases} \dfrac{V_A - V_B}{\omega L_t}\theta & 0 < \theta < \theta_a \\ \dfrac{-V_B}{\omega L_t}(\theta - \theta_a) + i_{Lt}(\theta_a) & \theta_a < \theta < \theta_b \\ 0 & \theta_b < \theta < \theta_c \end{cases} \tag{5.15}$$

Using Fig. 5.7 and (5.15), the transferred power P_{uc} when $V_A > V_B$ and the BDC in UCDM is

$$P_{uc} = \frac{V_A(V_A - V_B)\theta_a^2}{2\pi\omega L_t} \tag{5.16}$$

By applying the volt-second balance principle across the L_t during the first half-cycle, θ_a in relation to θ_b can be obtained as:

$$\theta_a = \frac{V_B}{(V_A - V_B)}\theta_b \tag{5.17}$$

where θ_b is

$$\theta_b = 2\varphi \tag{5.18}$$

where φ is imposed with respect to the central axis of the voltage pulse across the primary and secondary.

Then, the transferred power P_{uc}^{TRM} in relation to φ when $V_A > V_B$ is given as

$$P_{uc}^{TRM} = \frac{2\varphi^2 V_A V_B^2}{\pi\omega L_t (V_A - V_B)} \tag{5.19}$$

At the maximum power possible with the TRM the sum of θ_a and θ_b is equal to the duration of one half-cycle π and the period $\theta_c = 0$[9]. Hence, the period θ_b is equal to (π - θ_a). Based on that, the maximum phase-shift φ_{max}^{TRM} that maintains a triangular shape for the primary current and makes I(θ_b) equal to zero (see purple waveform in Fig. 5.7) is given as

$$\varphi_{max}^{TRM} = \frac{1}{2}\frac{\pi(V_A - V_B)}{V_A} \tag{5.20}$$

Substituting (5.20) in (5.19) the maximum power $P_{uc\_max}^{TRM}$ that can be transferred under TRM when $V_A > V_B$ and the BDC in UCDM is

$$P_{uc\_max}^{TRM} = \frac{\pi V_B^2}{2\omega L_t V_A}(V_A - V_B) \tag{5.21}$$

From (5.21), it is obvious that

$$P_{uc_{max}}^{TRM} = \begin{cases} + & \text{for} \quad V_A > V_B \\ 0 & \text{for} \quad V_A = V_B \\ - & \text{for} \quad V_A < V_B \end{cases} \tag{5.22}$$

Thus, when $V_A < V_B$ and $V_A = V_B$ the TRM cannot be used. TRM only permits a positive power transfer when $V_A > V_B$ and the BDC is in UCDM. Thus, the BDC operating under TRM requires a higher transformer turns ratio n. Hence, n should be designed as

[9] Notice that the duration of the periods θ_b and θ_c are controlled by changing the duty cycle of the DC link bridge.

$$n > \frac{V_o}{V_{uc\_min}} \tag{5.23}$$

High turns ratio means less power will be transferred by the BDC for the same φ.

The TRM operation with $V_A < V_B$ can be achieved if the $v_{pri}(t)$ and $v'_{sec}(t)$ waveforms are modified to be aligned at the falling-edge, as shown in Fig. 5.8. [137, 142]. In this case θ_a, θ_b and θ_c must be recalculated by driving the bridge switches with a duty cycle different from that used for $V_A > V_B$. This means further complexity added to the implementation of the switching control.

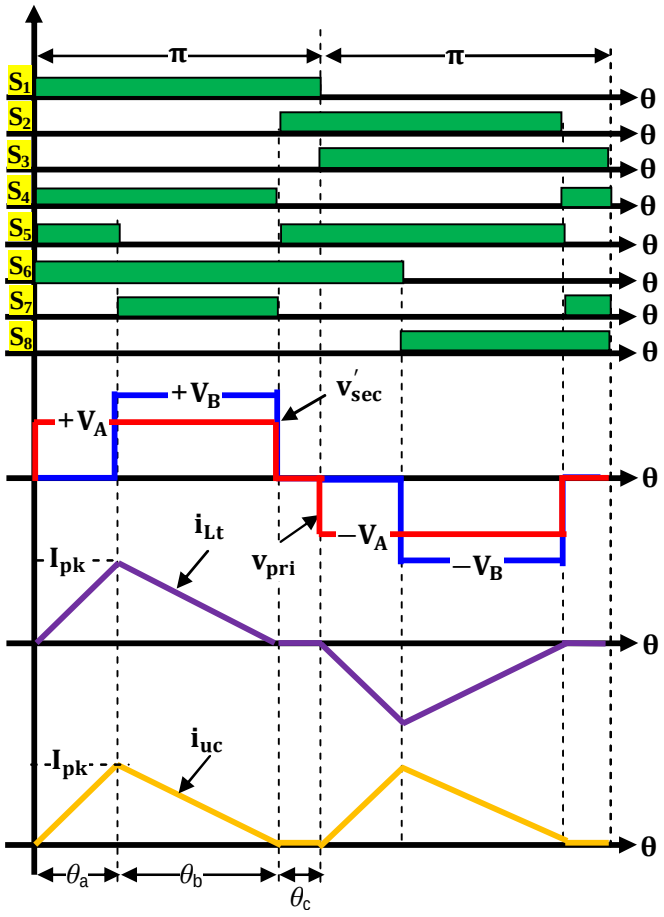


Fig. 5.8 Gate Signals, transformer voltages, primary current, and input current waveforms for TRM, when $V_A < V_B$ and the BDC in UDCM

5.3.2 Modified Triangular Current Modulation

To extend the range of the TRM operation so that can be used even when $V_A = V_B$, a modified TRM scheme called a "proposed TRM" (PTRM) was presented in [136]. As shown in Fig. 5.9, in this scheme the voltages V_A and V_B are arranged so there is no overlap. With the PTRM the primary current still keeps its triangular shape by selecting θ_a to be $\leq (\theta_b + \theta_c)$ over the entire load range. Hence, the primary current i_{Lt} during the periods θ_a, θ_b, and θ_c can be given as:

$$i_{Lt}(\theta) = \begin{cases} \dfrac{V_A}{\omega L_t}\theta & 0 < \theta < \theta_a \\ \dfrac{-V_B}{\omega L_t}(\theta - \theta_a) + i_{Lt}(\theta_a) & \theta_a < \theta < \theta_b \\ 0 & \theta_b < \theta < \theta_c \end{cases} \tag{5.24}$$

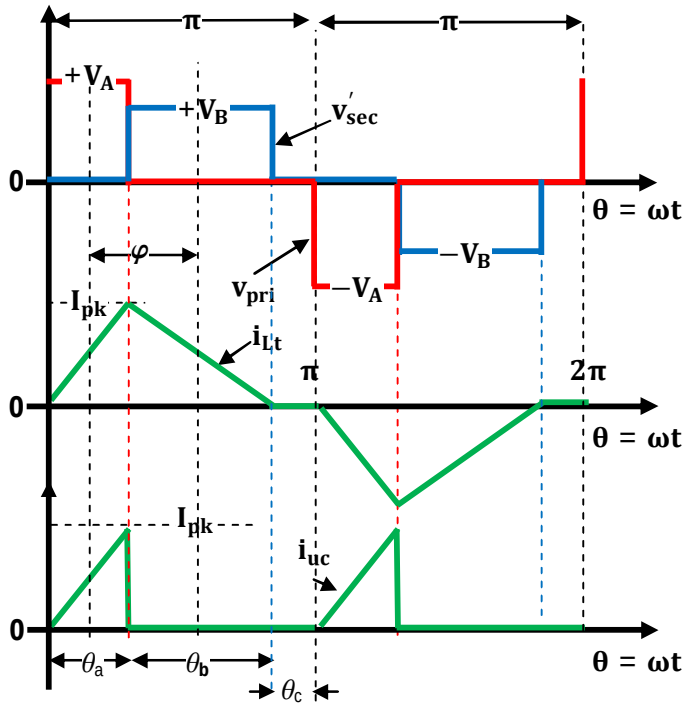


Fig. 5.9 Key waveforms of PTRM approach for $V_A > V_B$ with the BDC operating in UCDM

Using (5.24) and Fig. 5.9, the achievable transferred power by the PRTRM can be obtained as:

$$P_{uc}^{PTRM} = \frac{V_A^2 \theta_a^2}{2\pi\omega L_t} \tag{5.25}$$

From Fig. 5.9, the relation between θ_a, θ_b and φ (which is defined in Section 5.3.1) given as

$$\theta_b = 2\varphi - \theta_a \tag{5.26}$$

where

$$\theta_a = \frac{2\varphi V_B}{V_A + V_B} \tag{5.27}$$

Substituting (5.27) in (5.25), the transferred power P_{uc}^{PTRM} in relation to φ is

$$P_{uc}^{PTRM} = \frac{2\varphi^2 V_A^2 V_B^2}{\pi\omega L_t (V_A + V_B)^2} \tag{5.28}$$

Using the same procedure shown for TRM, the maximum phase-shift φ_{max}^{PTRM} and the maximum transferrable power $P_{uc\_max}^{PTRM}$ under PTRM are obtained as:

$$\varphi_{max}^{PTRM} = \frac{\pi}{2} = \theta_a = \theta_b \tag{5.29}$$

and

$$P_{uc\_max}^{PTRM} = \frac{\pi V_A^2 V_B^2}{2\omega L_t (V_A + V_B)^2} \tag{5.30}$$

Unlike conventional TRM, it is clear from (5.30) that the PTRM scheme permits a positive power transfer for the UCDM for any V_A and V_B values. However, this scheme has the drawback of high RMS and peak currents and can therefore be used only at the light load.

A modified triangular current modulation (MTRM) is proposed in [19, 144]. In this method the duty cycles of both bridges are varied between 0 to 50% in related to the amount of the power P_{uc}. The key waveform of MTRM is shown in Fig. 5.10.

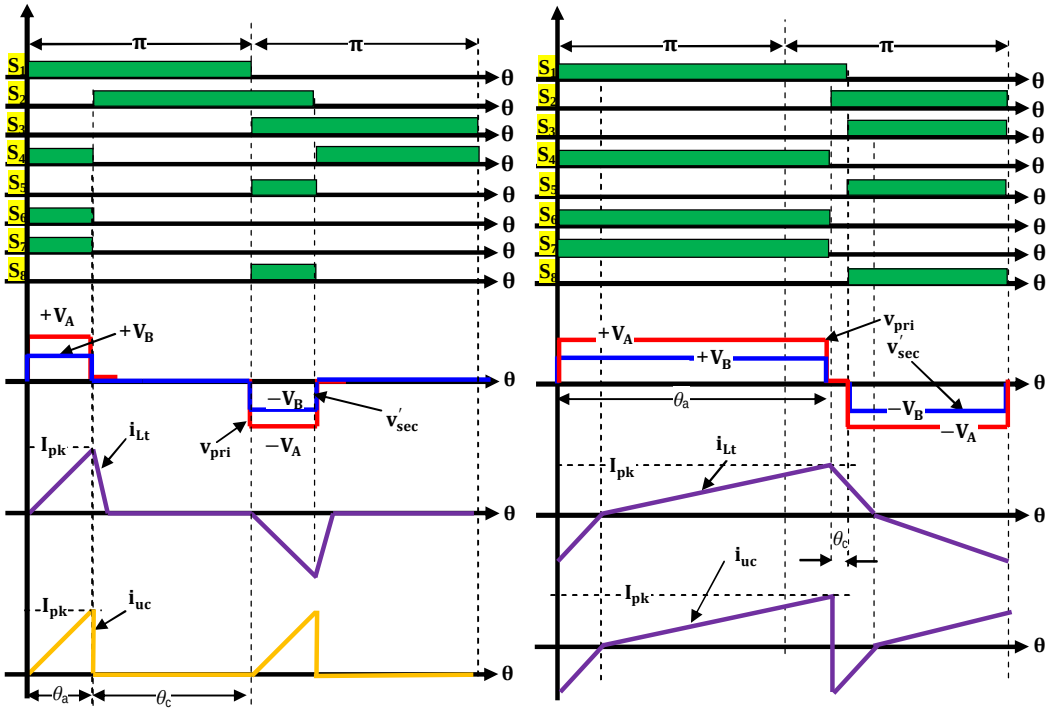


Fig. 5.10 Key waveforms of MTRM approach for $V_A > V_B$ with the BDC operating in UCDM

With MTRM, ZCS is realised for the UC bridge switches which reduces the circulating current. However, this is possible only at light load, as shown in Fig. 5.10b, and doesn't reduce the circulating current at the medium and high load .In addition it reduces the BDC power capability since it doesn't use a phase shift between the bridges but only change the RMS voltage across the bridges to control the power flow. Furthermore, asymmetrical voltage waveforms across the transformer can result in magnetic saturation of the transformer due to voltage–time imbalance.

5.3.3 Hybrid Modulation Schemes

With the TRM, PTRM, and MTRM the soft-switching operation range for the BDC can be significantly improved and the conduction loss reduced, but the penalty is that the maximum transferrable power is far below the maximum possible power of the BDC, making them undesirable for use in high power applications[10]. Therefore, several methods have been proposed in the literature to combine the above schemes with other modulations so that the full power capability of the BDC is exploiting. These methods described below:

A- PTRM-CPC Hybrid Modulation

A hybrid modulation for the BDC, based on a combination of a PTRM scheme (see Fig. 5.9) and CPC modulation (see Fig. 5.2), was presented in [136]. In PTRM-CPC the BDC operates with PTRM only for low power transfer while the CPC used for high power transfer, since the PTRM is not suitable for high power operation as mentioned before. Thus, with PTRM-CPC the BDC is operating under CPC for most of the power range, which is not preferable when the input voltage varies significantly, as indicated in Section 5.2. Furthermore, because the primary current is not zero at the transition from PTRM to CPC mode high peak currents could be incurred. Thus, to protect the BDC from high peak current at the mode transition a hysteresis comparator is required.

B- TRM-TZM Hybrid Modulation

In [127, 137, 142] a combination of TRM with the trapezoidal current modulation (TZM) is proposed. In this method the BDC is operating under TRM up to half-load

[10] Using these schemes at high power increases the peak current stress and the conduction loss in the BDC switches, thus reducing the efficiency.

after which TZM is employed. The key waveform of the TZM scheme is depicted in Fig. 5.11.

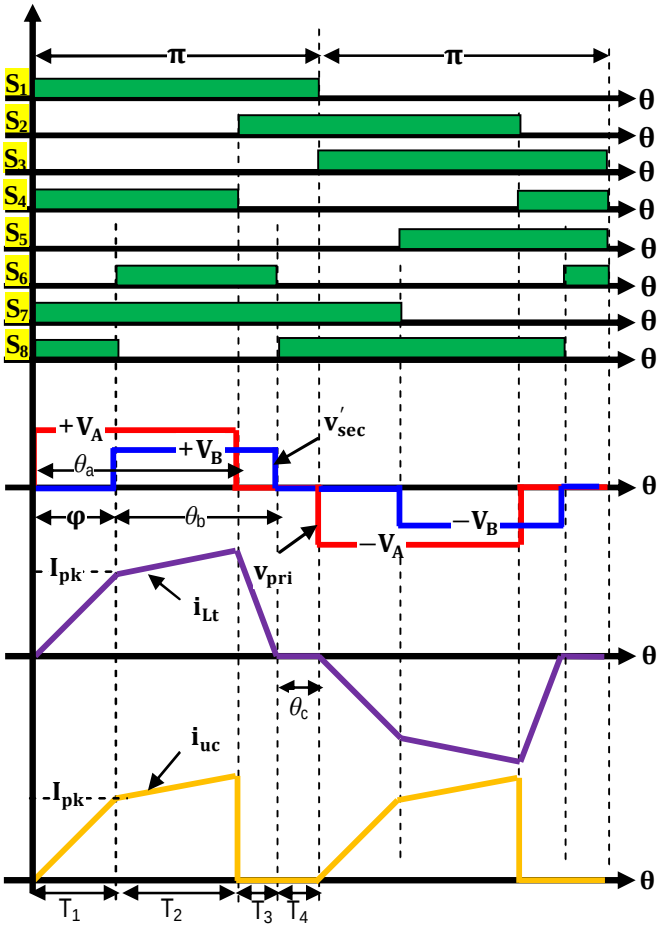


Fig. 5.11 Key waveforms of TZM approach for V_A>V_B with the BDC operating in UCDM

The operational modes of the BDC under the TZM scheme can be divided into 8 intervals over one switching cycle, as shown in Fig. 5.11. Compared to the CPC (see Fig. 5.2c), TZM imposed zero current through the transformer by applying a zero voltage across both bridge sides during the interval T_4. The primary current $i_{Lt}(\theta)$ during the first half-cycle (i.e. T_1, T_2, T_3 and T_4) when $V_A > V_B$ and the BDC operates under the UCDM can be given as

$$i_{Lt}(\theta) = \begin{cases} \frac{V_A}{\omega L_t}\theta & \text{for all } \theta \in T_1 \\ \frac{V_A - V_B}{\omega L_t}(\theta - \varphi) + i_{Lt}(\varphi) & \text{for all } \theta \in T_2 \\ \frac{-V_B}{\omega L_t}(\theta - \theta_a) + i_{Lt}(\theta_a) & \text{for all } \theta \in T_3 \\ 0 & \text{for all } \theta \in T_4 \end{cases} \quad (5.31)$$

Using (5.31) the transferred power that can be delivered by the BDC under TZM is given as

$$P_{uc}^{TZM} = \frac{V_A}{2\pi\omega L_t}(V_A\theta_a^2 - V_B(\varphi - \theta_a)^2) \quad (5.32)$$

With the TRM-TZM hybrid modulation the efficiency of the BDC is considerably improved compared to the PTRM-CPC hybrid modulation but the current through the primary winding becomes discontinuous over the entire power range which is not appropriate in most applications due to the higher device current stresses. In addition, the maximum power achieve by the BDC under the TRM-TZM is less than the maximum power capability of the CPC and the PTRM- CPC modulations.

C- TRM-TZM-CPC Combination

Further efficiency enhancements were developed by a combination of TRM, TZM, and CPC modulation schemes so that the appropriate scheme is selected based on the required output power [122]. Compared to the TRM-TZM hybrid modulation, combine TRM and TZM with the CPC modulation increases the power capability of the BDC and makes the efficiency much flatter over the entire range. However, the transition between the TZM (for a medium power operation) and the CPC (for a high power operation) caused a high spike current which increases the complexity of the controller significantly.

D- Composite dual PWM Scheme

To realize ZVS down to light-load and to reduce circulating energy, a composite scheme based on selecting either dual PWM for the low power transfer operation or a single PWM for the high power transfer operation is presented in [145]. For the high power transfer the BDC operates such as the modulation proposed in [141], where PWM used in addition to the CPC modulation. Using this scheme, maximum efficiency occurs only in the light load range.

In addition to the above several modulations and combination methods, other modulations have been proposed so that achieve a lower switching losses based on optimum selection of the duty cycles in respect to the phase-shift angle, such as in [139] [146-148]. Based on the BDC loss model, an accurate mathematical analysis has been achieved in [139] to calculate the required phase-shift angle and the duty cycle that result in minimisation of the peak currents and switching losses in the converter. However, this modulation require a very complex algorithm controller to generate the required phase-shift and duty cycle especially when the input and the output sources have wide voltage variation. In addition, it does not reduce the circulating energy and it restricts the converter power capability.

5.3.4 Voltage-Balance Modulation Scheme

Reference [146] proposes a duty ratio control modulation called as a volt-seconds balance control VBC modulation[11] to improve the soft-switching operation of the BDC. In this method the duty cycle D has been calculated in respect to the UC voltage as

[11] The main idea of the VBC modulation is to maintain the volt-second products across the transformer winding equal so that extending the ZVS range of the BDC switches

$$D = \frac{V_{uc\_min}}{2V_{uc}} \tag{5.33}$$

where V_{uc_min} = 50% of V_{uc}

Notice that V_{uc_min} and V_{uc_max} are the minimum and maximum UC voltage. This means that D = 50% if $V_{uc} = V_{uc\_min}$, and D = 25% if $V_{uc} = V_{uc\_max}$. This choice for duty cycle can provide ZVS for the ultracapacitor bridge side but only for a limited load range. Furthermore, if $V_{uc} = V_{uc\_min}$ the BDC has to be operated under CPC for the full power range. Also, the effect of the conduction losses and circulating energy is not addressed.

5.4 Comparison of Modulation Schemes and Conclusions

To control the power flow of the ultracapacitor bidirectional converter a phase-shift between the voltages across both sides of the converter is required. Despite the simplicity of implementation of this method, it causes degradation in the performance and operating efficiency of the converter. Therefore, an alternative modulation method to improve the converter performance is necessary. A number of modulation methods that have been proposed in the literature to control the power flow of the BDC with extended soft-switching operation and lower conduction losses are presented in this Chapter. Based on this detailed comparison, a new modulation has been proposed in the next Chapter.

Table 5.2 summarised the main features of different APM schemes described in this section.

TABLE 5.2
COMPARISON BETWEEN DIFFERENT APM SCHEMES

APM Scheme	RMS Current in the BDC	SSW Status	Power transfer Capability P_{uc_max}	Switching Controller Complexity	Limits
CPC	High	ZVS for all switches (only if $V_A=V_B$)	High (under the BDC power rating)	Very Low (Fixed duty cycle with variable phase-shift)	
TRM	Low (if operating with power rating less than TZM range)	ZVS and ZCS for all switches	Low (less than the achievable power of TZM), where the maximum power $P_{uc\_max}^{TRM}$ that can be transferred is $P_{uc\_max}^{TRM} = \frac{\pi V_B^2}{2\omega L_t V_A}(V_A - V_B)$	Very high (Variable duty cycle with phase-shift) (rising-edge and falling edge alignment required)	Doesn't work if $V_A= V_B$ and $V_A< V_B$ High n required
PTRM	Low (if operating under light load)	ZCS for all switches	Medium (higher than TRM and less than TZM when $P_{uc\_max}^{PTRM} = \frac{\pi V_A^2 V_B^2}{2\omega L_t (V_A+V_B)^2}$	High (Variable duty cycle with variable phase-shift)	Limits the duty cycle for both bridges to less than 25%
MTRM	Medium (at the light load) High (for the high power transfer)	ZCS for all switches when BDC operating under light load only	Medium	Medium (Variable duty cycle with fixed phase-shift)	
TZM	Lower than CPC within same operating range Higher than TRM	ZVS and ZCS for all switches	High but $<P_{uc\_max}^{CPC}$	High (Variable duty cycle with phase-shift)	
VSB	Medium if $V_{uc}> V_{uc\_min}$ High if $V_{uc}= V_{uc\_min}$	ZVS if $V_{uc}> V_{uc\_min}$	High only if $V_{uc}= V_{uc\_min}$	Medium (Variable duty cycle with phase-shift only if $V_{uc}> V_{uc\_min}$)	High n required

Chapter Six

New Modulation Scheme for an UC Bidirectional DC-DC Converter

6.1 Introduction

According to Chapter 5 the BDC with an IGBT voltage-doubler circuit provides twice the voltage conversion ratio, thus reducing the transformer turns ratio, and reduces the number of active devices. However, the voltage-doubler arrangement somewhat restricts the modulation scheme that can be used on the high-voltage side. For example, using the voltage-doubler zero volt across the secondary is not possible. Thus, to extend the SSW operation and reduce the RMS current a limited range of optimal operating points can be obtained. In order to improve the SSW range of the voltage-doubler switches further, an asymmetric duty cycle[1], as described in [140, 149], could be used for the voltage–doubler switches Z_1 and Z_2. But this would result in imbalanced current stresses in the switches and an asymmetrical voltage across the secondary winding.

On the other hand, by looking to aforementioned APM methods (in Section 5.3), it can be concluded that with those methods the price to pay in order to reduce the circulating current and extend the SSW operation is a discontinuous primary current, which is not appropriate in practical applications since it brings a higher peak and RMS current impact. In addition, to implement these modulations a complex control algorithm is required since these methods propose changing both the duty-cycle and the phase-shift

[1] Using this modulation an asymmetry between the on and off period of the secondary PWM signals is imposed.

of the gate signals. Also, some of these methods such as the TRM work only over a certain input voltage range, whilst other methods require a higher turns ratio such as the VPC modulation. Furthermore, all those methods are applicable only to BDC topologies with two H-bridges (see Fig. 5.6).

Moreover, unlike the converters for the high-input voltage applications, reducing the switching losses for the BDC operating with a low–voltage high–current source, such as the UC energy buffer, does not lead to considerable increasing in the converter efficiency. Since the conduction loss in the MOSFET is a function of the square of the RMS current, they will be the dominant losses that have a major impact on the converter efficiency.

To control the power flow of the presented BDC with an IGBT voltage-doubler circuit (Fig. 5.1) with minimum circulating power flow (see Section 6.4), minimum RMS current , and with SSW operation over the entire input voltage range, a new optimal modulation scheme is proposed in this Chapter. The proposed modulation can maintain a minimum circulating power flow even if the UC voltage is reduced to 58% of the rated voltage. The proposed optimal modulation scheme has been implemented based on the development of the switch control strategy for the BDC with voltage-doubler, as described in the next section. The modulation method is supported by a comprehensive mathematical analysis, and the correctness of the analysis has been validated by the detailed simulation using the SLPS-PIL dual co-simulation (see Section 6.5).

6.2 Switching Control Strategy and Design Considerations

6.2.1 Switching Control Strategy

To simplify implementation of the control algorithm for the BDC switches, an adapted

switch control strategy is proposed in this section. The switch control modifies the primary voltage only by overlap of the top/bottom switches of the UC bridge side for a specific period, by inserting a phase-shift angle (φ_2) between S_1 and S_3 (or S_2 and S_4) whilst maintaining a fixed 50% duty cycle, as shown in Fig. 6.1.

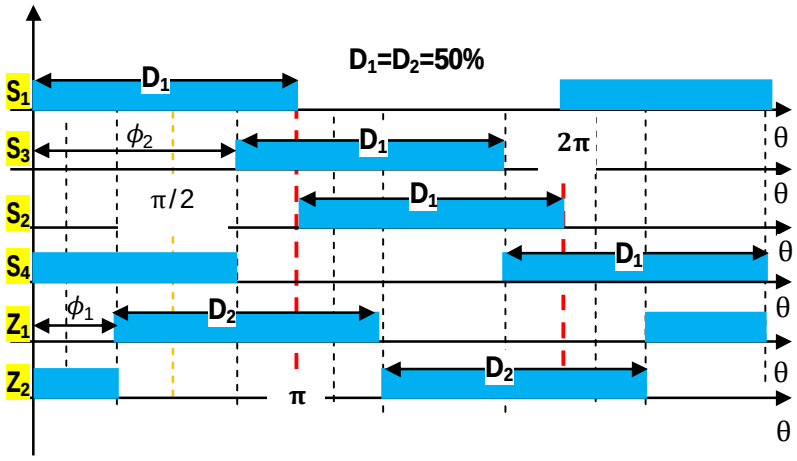


Fig. 6.1 Key waveforms of switch control strategy for the BDC with the IGBT voltage-doubler circuit with fixed duty cycles D_1 and D_2

The phase-shift angle φ_2 is named here the inner phase-shift[2]. The switching of S_2 and S_4 is complementary to that of S_1 and S_3 respectively. Switch Z_1 lags or leads the switch S_1 by a phase-shift φ_1 depending on the power flow direction. This method will facilitate implementation of the switching controller since no duty cycle variation is required.

6.2.1.1 Range of Phase-Shift φ_1 and φ_2

With the investigated BDC in Fig. 5.1, using the developed switch control five possible operating modes can be distinguished in respect to the phase-shift angles φ_1 and φ_2 when the BDC is operating under UCDM[3]: Mode I: $0^0 \le \varphi_1 \le 90^0$ and $0^0 \le \varphi_2 \le 90^0$ with condition $\varphi_1 = \varphi_2$; Mode II: $0^0 \le \varphi_1 \le 90^0$ and $0^0 \le \varphi_2 \le 90^0$ with condition $\varphi_1 \le \varphi_2/2$; Mode III: $90^0 \le \varphi_1 \le 180^0$ and $90^0 \le \varphi_2 \le 180^0$; Mode IV : $90^0 \le \varphi_1 \le 180^0$ and $0^0 \le \varphi_2 \le$

[2] Since the phase-shift φ_2 is between gates (or switches) of the same bridge.
[3] Similar phase-shift ranges can be achieved when BDC operating under UCCM.

90^0, and Mode V: $0^0 \leq \varphi_1 \leq 90^0$ and $90^0 \leq \varphi_2 \leq 180^0$ with condition $\varphi_1 \leq \varphi_2/2$. In order to discover the optimum phase-shift range that results in the lowest RMS current and switching losses, the performance of the BDC has been examined for each mode after which the selected operating range is used to implement the proposed optimal modulation scheme as will be introduced in Section 6.4.

The operating waveforms of the different φ_1 and φ_2 ranges are indicated in Fig. 6.2 a-e. All operating modes are discussed here with respect to the power capability of the BDC, SSW operation, and primary RMS current $i_{Lt}(\theta)$.

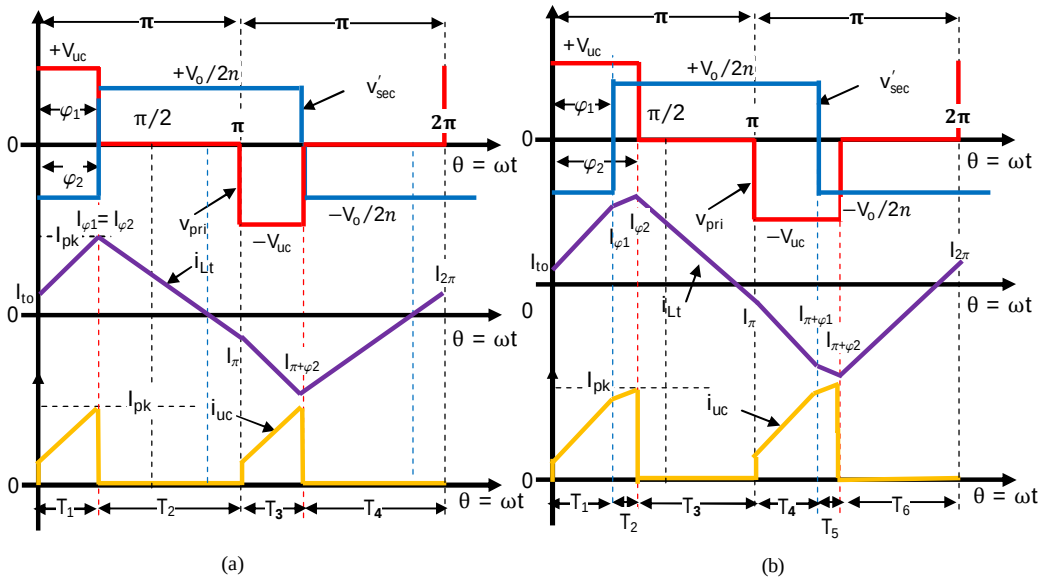
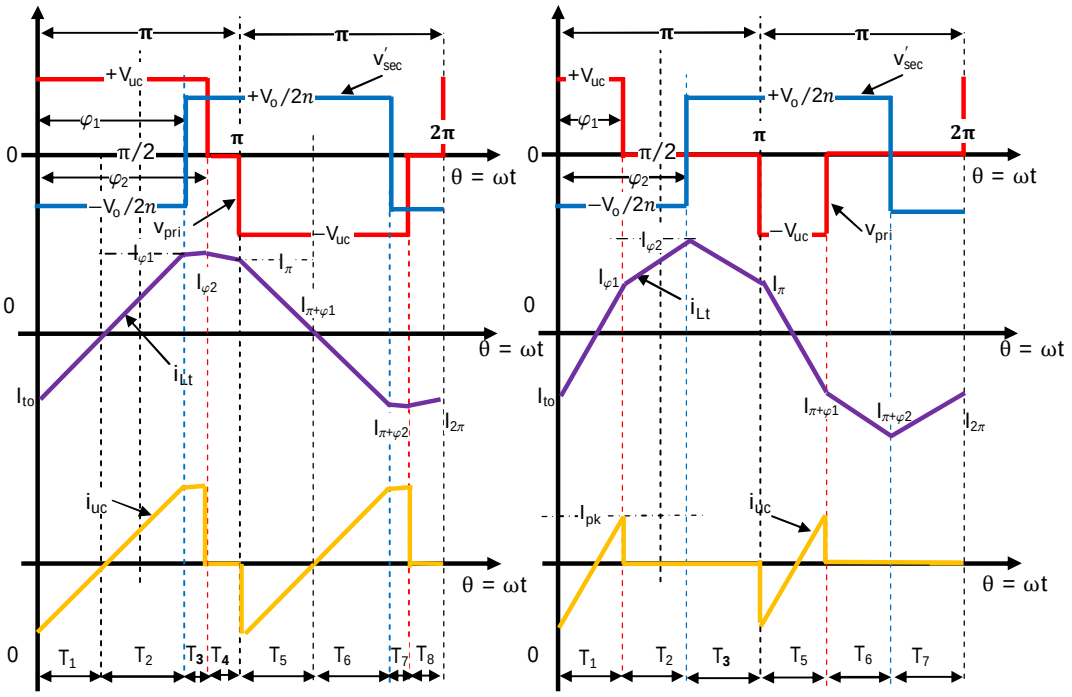


Fig. 6.2 Possible operation modes at different phase-shift angles φ_1 and φ_2 ranges under UCDM
(continued on the next page)



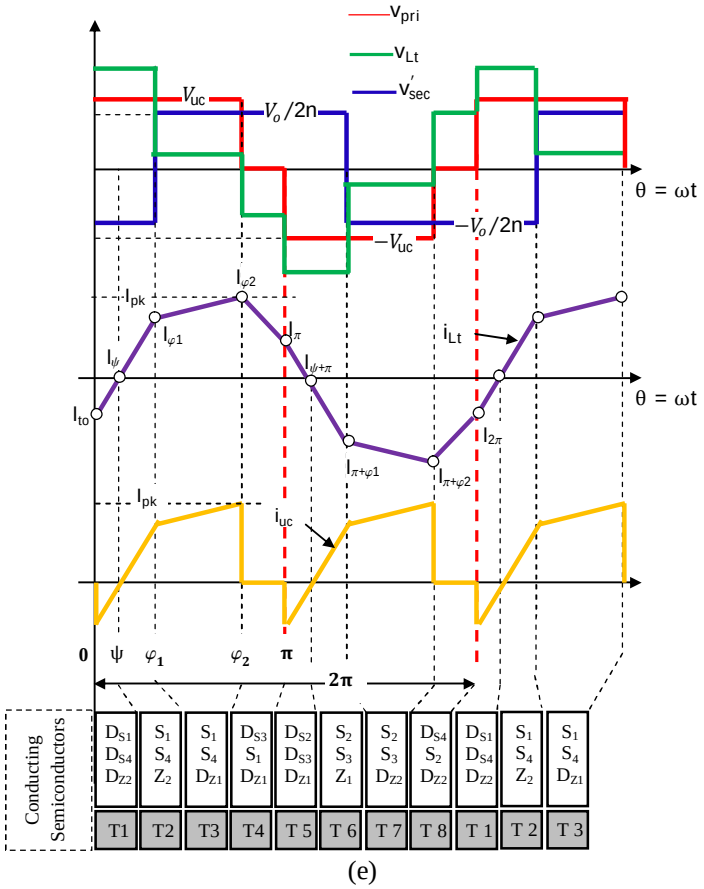


Fig. 6.2cont.: Possible operation modes at different phase-shift angles φ_1 and φ_2 ranges under UCDM: (a) Mode I: $0^0 \le \varphi_1 \le 90^0$, $0^0 \le \varphi_2 \le 90^0$ with $\varphi_1=\varphi_2$, (b) Mode II: $0^0 \le \varphi_1 \le 90^0$, $0^0 \le \varphi_2 \le 90^0$ with $\varphi_1 \le \varphi_2/2$, (c) Mode III: $90^0 \le \varphi_1 \le 180^0$, $90^0 \le \varphi_2 \le 180^0$, (d) Mode IV: $90^0 \le \varphi_1 \le 180^0$, $0^0 \le \varphi_2 \le 90^0$, and (e) Mode V: $0^0 \le \varphi_1 \le 90^0$, $90^0 \le \varphi_2 \le 180^0$ with $\varphi_1 \le \varphi_2/2$. The operation intervals of the Mode V are T_1: $(0 \le \theta \le \psi)$, T_2: $(\psi \le \theta \le \varphi_1)$, T_3: $(\varphi_1 \le \theta \le \varphi_2)$, T_4: $(\varphi_2 \le \theta \le \pi)$, T_5: $(\pi \le \theta \le \pi + \psi)$, T_6: $(\pi + \psi \le \theta \le \pi + \varphi_1)$, T_7: $(\pi + \varphi_1 \le \theta \le \pi + \varphi_2)$, T_8: $(\pi + \varphi_2 \le \theta \le 2\pi)$

The expression of the primary current $i_{Lt}(\theta)$ for each Mode are given in (6.1) to (6.3) while the values of the currents I_{to}, $I_{\varphi 1}$, $I_{\varphi 2}$, I_{π}, $I_{\pi+\varphi 1}$, and $I_{\pi+\varphi 2}$, at the commutation instants 0, φ_1, φ_2 , π, $\pi+\varphi_1$, and $\pi+\varphi_2$ are given in Table 6.1.

Mode I:

$$i_{Lt}(\theta) = \begin{cases} \dfrac{V_o + 2nV_{uc}}{2n\omega L_t}\theta + i_{Lt}(0) & \theta \in T_1 \\ -\dfrac{V_o}{2n\omega L_t}(\theta - \varphi_2) + i_{Lt}(\varphi_2) & \theta \in T_2 \end{cases} \tag{6.1}$$

Modes II, III and V:

$$i_{Lt}(\theta) = \begin{cases} \dfrac{V_o + 2nV_{uc}}{2n\omega L_t}\theta + i_{Lt}(0) & \theta \in T_1^{\blacksquare} \\ \dfrac{(2nV_{uc} - V_o)}{2n\omega L_t}(\theta - \varphi_1) + i_{Lt}(\varphi_1) & \theta \in T_2^{\blacksquare} \\ \dfrac{-V_o}{2n\omega L_t}(\theta - \varphi_2) + i_{Lt}(\varphi_2) & \theta \in T_3^{\blacksquare} \end{cases} \tag{6.2}$$

where $T_1^{\blacksquare}$, $T_2^{\blacksquare}$, and $T_3^{\blacksquare}$ in Mode II are equal to T_1, T_2, T_3 respectively, while in Modes III and V they are equal to T_1+T_2, T_3, and T_4 respectively.

Mode IV:

$$i_{Lt}(\theta) = \begin{cases} \dfrac{V_o + 2nV_{uc}}{2n\omega L_t}\theta + i_{Lt}(0) & \theta \in T_1 \\ \dfrac{V_o}{2n\omega L_t}(\theta - \varphi_1) + i_{Lt}(\varphi_1) & \theta \in T_2 \\ \dfrac{-V_o}{2n\omega L_t}(\theta - \varphi_2) + i_{Lt}(\varphi_2) & \theta \in T_3 \end{cases} \tag{6.3}$$

TABLE 6.1
EXPRESSIONS OF THE CURRENT VALUES AT THE COMMUTATION INSTANTS FOR OPERATING MODES WHEN BDC IS UNDER UCDM OPERATION

Current Values	Mode I	Mode II, III and V	Mode IV
I_{to}	$\frac{\pi V_o - 2V_o\varphi_2 - 2nV_{uc}\varphi_2}{4n\omega L_t}$	$\frac{V_o(\pi - 2\varphi_1) - 2nV_{uc}\varphi_2}{4n\omega L_t}$	$\frac{(\pi - 2\varphi_2)V_o - 2nV_{uc}\varphi_1}{4n\omega L_t}$
$I_{\varphi 1}$	$I_{\varphi 2}$	$\frac{\pi V_o + 2nV_{uc}(2\varphi_1 - \varphi_2)}{4n\omega L_t}$	$\frac{\pi V_o + 2(V_o + nV_{uc})\varphi_1 - 2V_o\varphi_2}{4n\omega L_t}$
$I_{\varphi 2}$	$\frac{\pi V_o + 2nV_{uc}\varphi_2}{4n\omega L_t}$	$\frac{V_o(\pi + 2\varphi_1 - 2\varphi_2) + 2nV_{uc}\varphi_2}{4n\omega L_t}$	$\frac{\pi V_o + 2nV_{uc}\varphi_1}{4n\omega L_t}$
I_{π}	$-I_{to}$	$-I_{to}$	$-I_{to}$
$I_{\pi+\varphi 1}$	$I_{\pi+\varphi 2}$	$-I_{\varphi 1}$	$-I_{\varphi 1}$
$I_{\pi+\varphi 2}$	$-I_{\varphi 2}$	$-I_{\varphi 2}$	$-I_{\varphi 2}$

As indicated in Section 5.2, the BDC operates with ZVS when the stored energy in the series inductance is sufficient to discharge and charge the switch's parasitic capacitance. Hence, with the proposed switch control strategy the BDC switches operating with ZVS if the following conditions are realised

$$I_{to} < 0,\ I_{\varphi 1} > 0,\ I_{\varphi 2} > 0,\ I_{\pi} > 0,\ I_{\pi+\varphi 1} < 0,\ I_{\pi+\varphi 2} < 0 \qquad (6.4)$$

In Modes I and II, operation with ZVS is possible for all voltage-doubler switches while the switches of the leading leg of the UC-bridge cannot turn on with zero volts in these modes (see Fig. 6.2 a and b). In contrast, Modes III, IV, and V satisfy the ZVS conditions for the UC-bridge and voltage-doubler switches (see Fig. 6.2c-e). In addition, it is clear from the waveforms of Modes I, II, and IV (see Fig. 6.2 a, b, and d) that the power transferred to the output ($P_{uc} = v_{pri} \times i_{uc}$), when v_{pri} and i_{uc} have the same polarity, is less than the circulating power (see Section 6.3) through the transformer

during the periods T_3 in Fig. 6.2a, T_2 in Fig. 6.2b and T_2+T_3 in Fig. 6.2d. Thus, operation the BDC in Modes I, II, and IV reduces the power capability of the BDC.

Using (6.1) to (6.3) and the equations in Table 6.1, the maximum power achieved by the BDC operating in Modes I, II, IV, and V under UCDM is shown in Table 6.2, where the following parameters have been used L_t=10µH, V_o= 650V; n=7.4, f_s=20kHz, V_{uc}= 48V.

TABLE 6.2
POWER CAPABILITIES OF THE BDC WITH DIFFERENT OPERATING MODES

Power P_{uc}	Mode I	Mode II	Mode III	Mode IV	Mode V
P_{max}	$\frac{\pi V_o V_{uc}}{16n\omega L_t}$ = 659W	$\frac{3\pi V_o V_{uc}}{32n\omega L_t}$ = 988W	$\frac{\pi V_o V_{uc}}{8n\omega L_t}$ = 1318W	$\frac{\pi V_o V_{uc}}{16n\omega L_t}$ = 659W	$\frac{\pi V_o V_{uc}}{8n\omega L_t}$ = 1318W

It can be seen from Table 6.2 that the converter can operate at the full power rating only in Modes III and V. Hence, Modes I and II and IV are undesirable since they are not able to deliver the required maximum power.

Again using (5.9), (6.1) to (6.3) and Table 6.1, an expression for the primary RMS current for the Modes I to V are obtained as[4]:

Mode I:

$$I_{rms} = \sqrt{\frac{\pi}{3}}\sqrt{\frac{P_{uc}^2(\pi^3 V_o^2 + 4nV_oV_{uc}(3\pi - 2\varphi_2)\varphi_2^2 + 4n^2V_{uc}^2(3\pi - 2\varphi_2)\varphi_2^2)}{V_o^2V_{uc}^2(\pi - \varphi_2)^2\varphi_2^2}} \quad (6.5)$$

[4] Notice that to quickly derive all the expressions in Chapter 5 and this Chapter the "Mathematica" software tool is used (an example of how this tool can be used is given in Appendix I). Of course, any other software tool, such as "Maple" will do the job, too. However, numerical programs (such as Matlab) are not suitable to deriving these equations. In particular, it will be extremely difficult to obtain (6.5)-(6.7) or the equations in Section 6.4 without using a software tool.

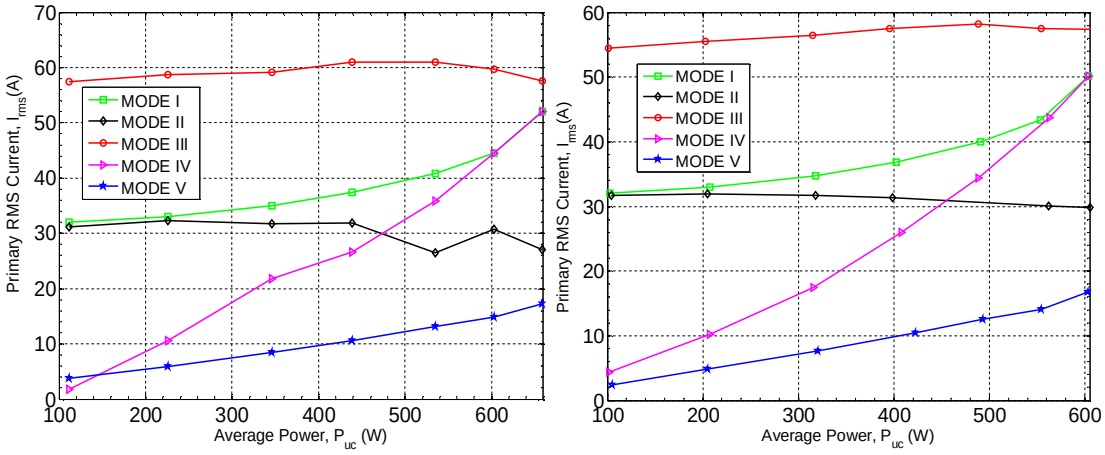
Modes II, III and V:

$$I_{rms} = \sqrt{\frac{\pi}{3}}\sqrt{\frac{P_{uc}^2(\pi^3V_o^2+4n^2V_{uc}^2(3\pi-2\varphi_2)\varphi_2^2-4nV_oV_{uc}(2\varphi_1-\varphi_2)(2\varphi_1^2-2\varphi_1\varphi_2+\varphi_2(-3\pi+2\varphi_2)))}{V_o^2V_{uc}^2(2\varphi_1^2-2\varphi_1\varphi_2+\varphi_2(\varphi_2-\pi))^2}} \quad (6.6)$$

Mode IV

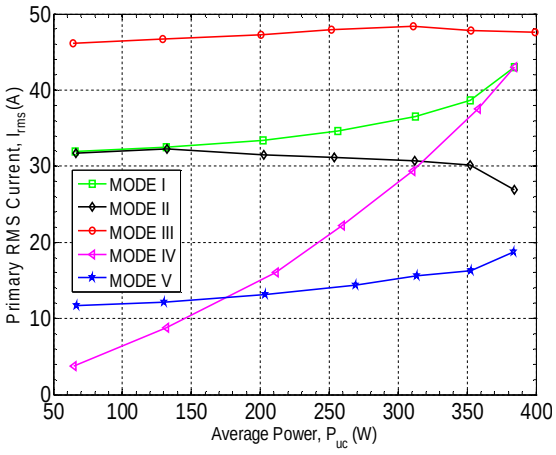
$$I_{rms} = \sqrt{\frac{\pi}{3}}\sqrt{\frac{P_{uc}^2(\pi^3V_o^2+4n^2V_{uc}^2(3\pi-2\varphi_1)\varphi_1^2-4nV_oV_{uc}\varphi_1(2\varphi_1^2+3\varphi_1(\pi-2\varphi_2)+6\varphi_2(-\pi+\varphi_2)))}{V_o^2V_{uc}^2\varphi_1^2(\pi+\varphi_1-2\varphi_2)^2}} \quad (6.7)$$

Using the parameters in Appendix J (Table J.1, Table J.2, and Table J.3) the calculated primary RMS currents for different operating Modes and different UC voltage levels are plotted in Fig. 6.3a-c.



(a) (b)

Fig. 6.3 The resulting primary RMS current of the BDC operating with different modes under UCDM
(continued on the next page)



(c)

Fig. 6.3cont. The resulting primary RMS current of the BDC operating with different modes under UCDM (L_t=10µH, V_o= 650; n=7.4; f_s=20kHz) for (a) V_{uc} = 48V, (b) V_{uc} = 44V (i.e. $2nV_{uc} = V_o$), and (c) V_{uc} = 28V

In addition to the reduced power capability of the BDC in Modes I, II, and IV, these modes in addition to Mode III results in increased RMS values of the primary current as shown in Fig. 6.3a-c (green, black, pink, and red lines respectively).

As indicated in Table 6.2, Mode III is capable to make the BDC operates with a maximum power range, but it is clear from Fig. 6.3 (red lines) that in this Mode the BDC is operating with high RMS current even at the light load. As stated in Section 5.2 (and see Section 6.3.1 as well), it is preferable for the BDC to operate with a small phase-shift φ_1 in order to reduce the circulating current, thus minimise the RMS current and conduction losses. Unfortunately, Mode III operates with a large phase-shift angle φ_1 for the same power of the other modes. Hence, operation in Mode III is undesirable.

It can be seen from Fig. 6.3a-c that RMS current is lowest in Mode V(blue lines) and this mode doesn't result in a reduced BDC power level as shown in Table 6.2. For P_{uc} = 440W and V_{uc} = 48V the primary RMS current is only 10.6A in Mode V compared to 37.5A in Mode I, 31.8A in Mode II, 60A in Mode III, and 26.6A in Mode IV. Thus, a considerable improvement can be achieved if Mode V is used.

6.2.1.2 Mode V Operation

A- RMS Current Analysis

As described in the last Section, an investigation for different operating modes was undertaken to find an optimum operating ranges for the phase-shifts φ_1 and φ_2 that result in the lowest RMS current and switching losses. In Mode V, when $0^0 \leq \varphi_1 \leq 90^0$ and $90^0 \leq \varphi_2 \leq 180^0$, a minimum RMS current and conduction losses can be achieved whatever the UC voltage value is (see Fig. 6.3a-c). However, Fig. 6.3 (blue lines) are plotted for arbitrary φ_1 and φ_2, thus the selection of φ_1 and φ_2 is not the optimal choice that lead to the lowest circulating current and RMS current at the same average power.

To clarify that, the primary RMS current with the full range of the phase-shift φ_1 and φ_2 is portrayed in Fig. 6.4 when P_{uc} =130W and 600W with two different UC voltage V_{uc}= 28V and 48V respectively. It is clear that a lower RMS current can be obtained at the same power for a certain angles of φ_1 and φ_2. For example, as shown in Fig. 6.3c (blue line) at P_{uc} = 130W and V_{uc} =28V primary RMS current is 12A. However, a considerable lower primary RMS current of 5.2A (at the same value of V_{uc} and P_{uc}) can be obtained as shown in Fig. 6.4a for different combination of φ_1 and φ_2. Same improvement can be observed in Fig. 6.4b, c, and d.

Similar to Mode V, lower RMS current values can also be achieved for the BDC when it is operating with Modes I, II, III, and IV. However, since Modes I, II, and IV results in reduction of the power capability of the BDC (see Section 6.2.1.1 and Table 6.2) they are not considered.

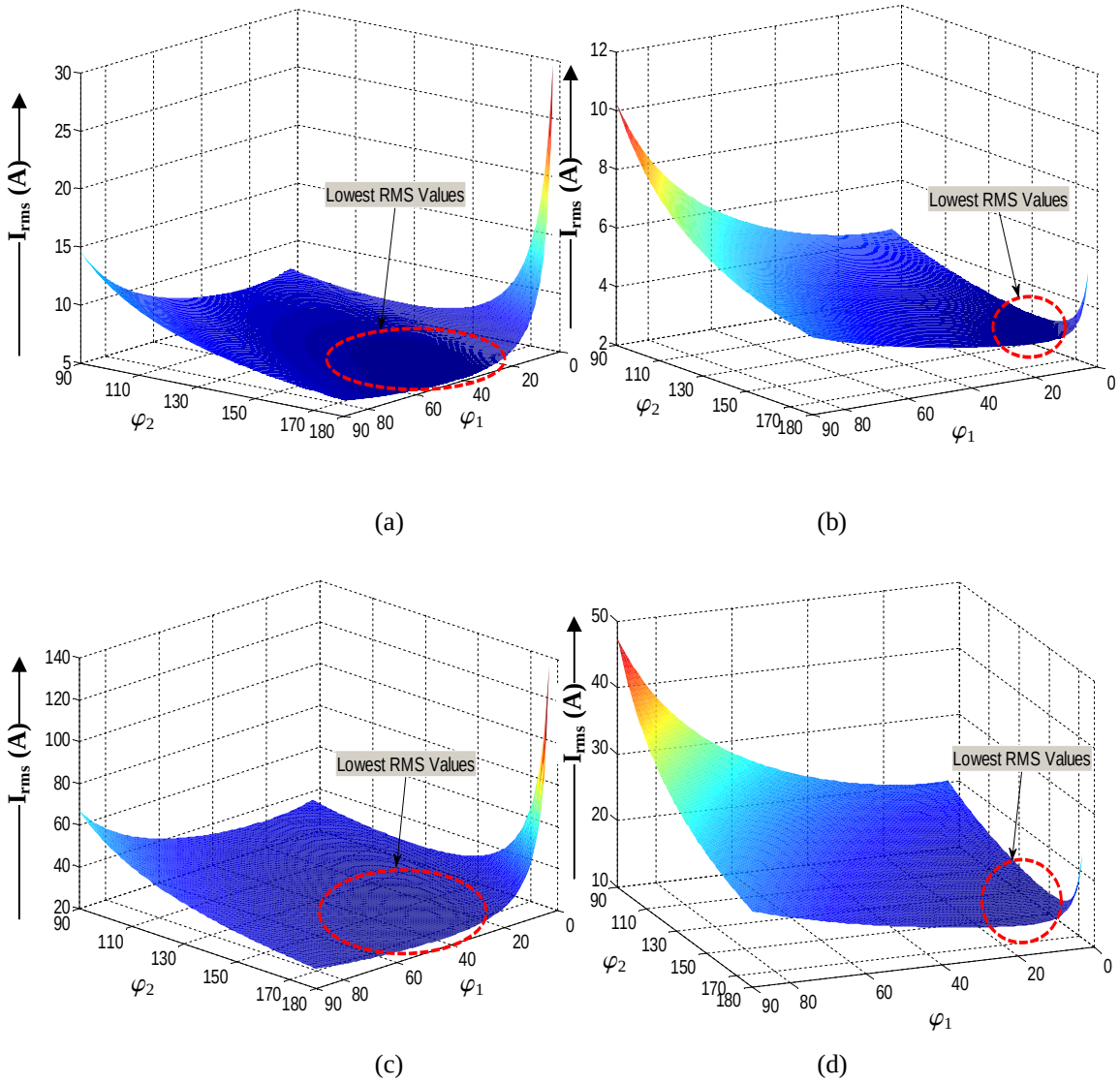


Fig. 6.4 Primary RMS current of the BDC operates with the Mode V for (a) P_{uc} =130W and V_{uc}=28V (b) P_{uc} =130W and V_{uc}= 48V (c) P_{uc} = 600W and V_{uc}= 28V and (d) P_{uc} = 600W and V_{uc}= 48V

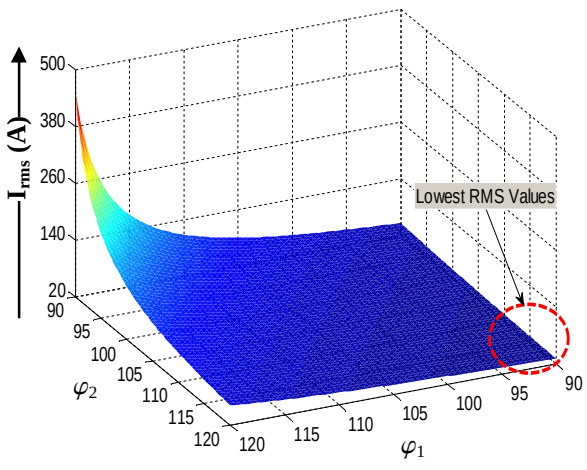


Fig. 6.5 Primary RMS current of the BDC operates with the Mode III for P_{uc} = 600W and V_{uc}= 48V

For the Mode III, the primary RMS current with different combination of φ_1 and φ_2 is depicted in Fig. 6.5. It can be seen that, for P_{uc} = 600W and V_{uc} = 48V, the RMS current is reduced to half (31A) of that in Fig. 6.3a (red line). However, the RMS current is still much higher than of Mode V (only 14A as indicated in Fig. 6.4d).

It would, of course, be preferable to find the optimum combination of φ_1 and φ_2 that leads to the lowest RMS current and thus increase the converter efficiency. But this would require a very complex algorithm to find the minimum RMS current. Hence, optimal modulation method is proposed here which is designed to achieve:

- Minimum circulating power flow in the BDC over the entire load range (see Section 6.3), which is the main criterion used in this work to improve the efficiency of the BDC.
- Low RMS currents to reduce the conduction losses
- ZVS and ZCS for UC-side and DC-link side to reduce the switching losses
- Simplify implementation of the control algorithm that selects the optimum combination of φ_1 and φ_2 in respect to minimum circulating power flow

With the use of the proposed method (as will be described later) efficiency improvements are achieved without increasing the complexity of the control algorithm or its implementation.

B- Power Transfer

Using the current and voltage waveforms in Fig. 6.2e (i.e. Mode V), the power transfer of the BDC for arbitrary φ_1 and φ_2 when $P_{uc} > 0$ (i.e. UCDM operation) can be found as:

$$P_{uc} = \frac{V_{uc}}{\pi}\left(\frac{1}{2}(I_{to} + I_{\varphi_1})\varphi_1 + \frac{1}{2}(I_{\varphi 1} + I_{\varphi_2})(\varphi_2 - \varphi_1)\right) \tag{6.8}$$

Substituting the expressions for the currents in Table 6.1 (third column), the average power P_{uc} can be described as:

$$P_{uc} = \frac{V_o V_{uc}}{4n\omega L_t}(-2\varphi_1^2 + 2\varphi_1\varphi_2 + (\pi - \varphi_2)\varphi_2) \qquad (6.9)$$

Fig. 6.6 shows the power flow contour surface of the BDC with voltage-doubler for both power flow directions, i.e. UCCM (bottom) and UCDM (top) operation. The yellow lines in both surfaces indicate the boundaries of the Mode V.

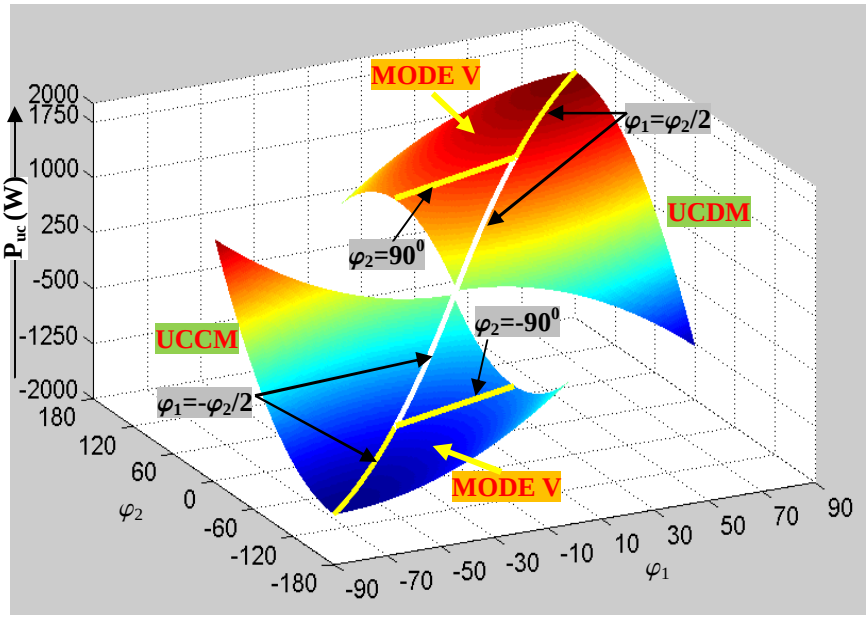


Fig. 6.6 3D contour surface of the BDC under UCDM (top surface) and UCCM (bottom surface): (n=7.4, L_t =10μH, V_{uc} = 48V, f_s =20kHz)

By setting the derivative $(\partial P_{uc}/\partial \varphi_1)$ of (6.9) to zero, the maximum phase-shift angle of φ_1 given as:

$$|\varphi_1| = \frac{|\varphi_2|}{2} \qquad (6.10)$$

where $90^0 \leq |\varphi_2| \leq 180^0$

Based on the above condition, the phase-shift angle φ_1 must be selected. Beyond this condition, the average power P_{uc} is reduced because of excessive power loss caused by

the circulating power flow (see Section 6.3). It is clear from the power flow characteristics of the BDC in Fig. 6.6 that the converter operates at the maximum power $P_{uc\_max}^{CPC}$ only when the CPC modulation is applied (i.e. when $\varphi_1 = 90^0$ and $\varphi_2 = 180^0$).

6.2.2 Design Considerations

The objective of the BDC is to interface the UC energy buffer to the DC link and manage the power flow between DC microgrid components. Even though the BDC is used for short periods of operation compared to the FC system it is contributing to the overall efficiency of the DC microgrid. Therefore, the converter parameters should be selected carefully in order to guarantee high operating efficiency. The series inductance L_t and the transformer turns ratio n are the main parameters that impact on the BDC efficiency.

According to (5.6), the power characteristic of the BDC under CPC modulation for different series inductance L_t values can be depicted as in Fig. 6.7.

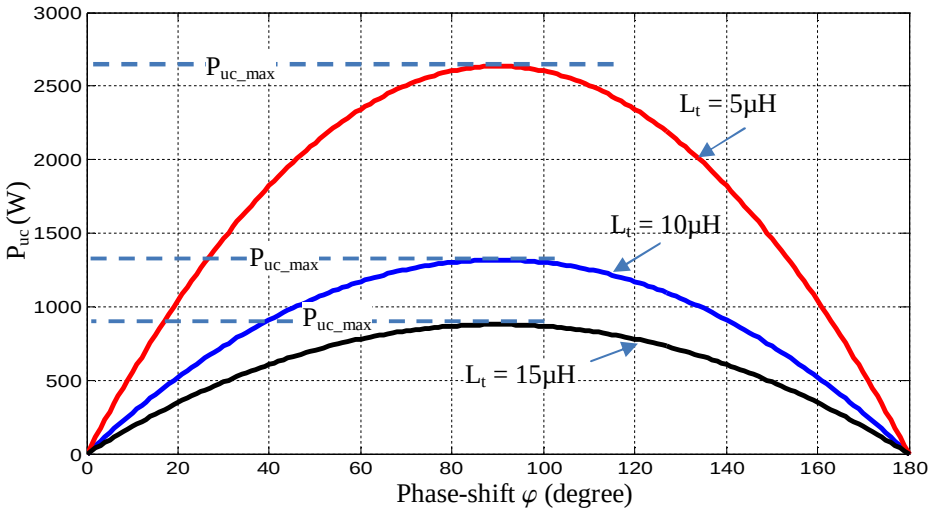


Fig. 6.7 BDC power flow against the phase-shift φ for different series inductance L_t values (V_{uc}=48V, f_s=20kHz, V_o=650V, n=7.4)

As can be seen the BDC can transfer more power with a smaller series inductance L_t. Also, it is can be seen that a smaller L_t reduces the required phase-shift angle for the same power P_{uc}. Thus, it is desirable to select a low series inductance L_t for the BDC.

But according to (5.10) and (5.11) the RMS current increases for a smaller series inductance L_t for the same values of the turns ratio n, UC voltage V_{uc}, and transferred power P_{uc}. Hence, a small inductance leads to an increase in the conduction losses and transformer copper losses since these losses are a function of I_{rms}^2, reducing the BDC efficiency. Furthermore, operation with the small phase-shift angle increases the sensitivity of the transferred power to the phase-shift and leads to the need for a high resolution control circuit. Based on that, the choice of the series inductance L_t is a trade-off between the required power, phase-shift angle, and the RMS current stress through the converter.

For the present low-voltage high-current application the conduction and copper losses outweigh the switching losses. To reduce these losses the RMS current should be minimised. Therefore, to limit the RMS currents via the converter's switches and transformer windings, an external inductance (L_{ext}) in series with the leakage inductance (L_σ) of the transformer is required, giving a total circuit inductance $L_t = L_{ext} + L_\sigma$ (in a practical converter, the transformer can be designed with an enlarged leakage inductance L_σ value close to the required external series inductance L_t to avoid the use of external inductance L_{ext}). According to (5.7), the required series inductance L_t should be chosen as

$$L_t \leq \frac{V_o V_{uc}}{16 n f_s P_{uc}} \tag{6.11}$$

With P_{uc} = 1.3kW, V_{uc} = 48V, V_o = 650V, n = 7.4, f_s=20kHz, this yields $L_t \cong 10\mu H$.

Notice that the series inductance L_t has been determined based on operation of the BDC under the CPC method. This is because this method is employed to provide the maximum power for the BDC when operating with the proposed optimal modulation scheme (see Section 6.4).

The second important parameter is the transformer turns ratio. If the BDC is using the standard voltage-fed configuration (see Fig. 5.1), a high turns ratio is mandatory. But a high turns ratio means more copper losses and a lower power flow. For the TRM and VBC methods are even higher turns ratio is required since they doesn't work with low input voltage (i.e. when $2nV_{uc} < V_o$).

On the other hand, with the voltage-doubler circuit the required turns ratio is only half of that for dual H-bridge BDC (Fig. 5.6). This reduces the copper losses, whilst increasing the voltage conversion ratio with the same power capability of the dual H-bridge BDC. Thus, for $V_{uc} = 44V$ and $V_o = 650V$ the required turns ratio ($n = V_o / 2V_{uc}$) is equal to 7.4.

In order for the converter to be able to deliver the rated power (i.e. 1.3kW) even at 24V, the converter should be oversized by 50% compared to 48V operation, with corresponding higher current stresses. To avoid this the current converter is designed for 1.3kW at 48V and 0.66kW at 24V.

6.3 Circulating Power Flow (CPF) Analysis

It is known that circulating power flow (CPF) or circulating energy in the converter has a major effect on increasing the conduction losses, thereby reducing the operating efficiency [150]. This power that occurs during a certain interval in the cycle depends on the used modulation scheme and varies with the load conditions. Therefore, the

definition and determination of this interval is first discussed in this section, after which a modulation scheme is investigated that provides a minimum CPF interval.

6.3.1 Definition of CPF Interval

Due to the series inductance L_t the primary and secondary currents lag their voltage by an angle that varies with the required power. Consequently, part of the absorbed power is circulating through the converter and flows back to the input source. This is shown in Fig. 6.8 (bottom waveform) for the BDC operating with CPC, where the instantaneous power across the primary $P_{pri}(\theta)$ is plotted for one full cycle of the converter operation for an arbitrary phase-shift angle φ. The interval denoted by ψ is defined here as the CPF interval and is related to the power required by the load. To find a mathematical equation representing the CPF interval, the absolute value of the primary current $|i_{Lt}(\theta)|$ waveform is also plotted in Fig. 6.8 (top waveform). For simplification, the waveforms are plotted for $2nV_{uc} = V_o$. Notice that the average value of the primary current $i_{Lt}(\theta)$ is equal to zero over the full-cycle. Thus, for the first half-cycle the current for each interval can be obtained as:

$$i_{Lt}(\theta) = \begin{cases} \dfrac{V_o}{n\omega L_t}\theta + I_{to} & 0 \le \theta \le \varphi \\ I_\varphi = I_\pi & \varphi \le \theta \le \pi \end{cases} \tag{6.12}$$

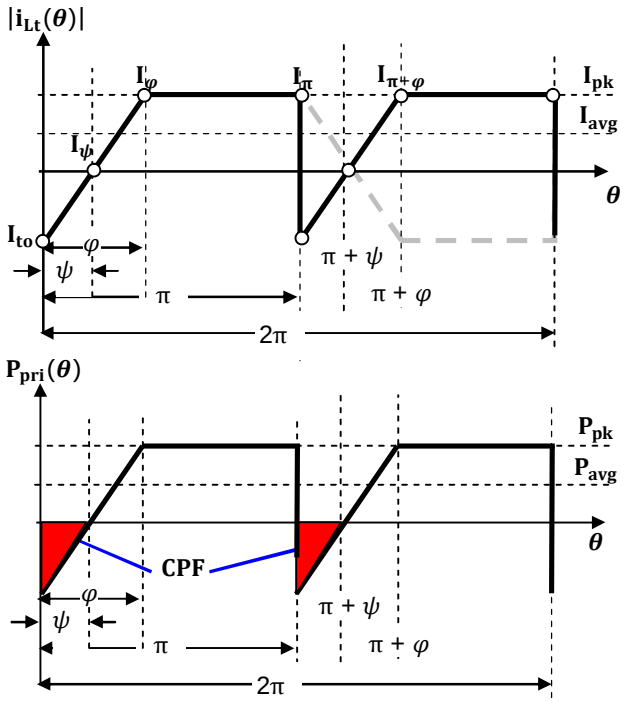


Fig. 6.8 Instantaneous power flow of the BDC measured across the primary side (P_{pri}) for $P_{uc} > 0$ plotted for arbitrary φ_1 and φ_2.

The values of the currents I_{to} and I_φ at the commutation instants 0 and φ are given as

$$I_{to} = -\frac{V_o}{2n\omega L_t}\varphi \tag{6.13}$$

and

$$I_\varphi = \frac{V_o}{2n\omega L_t}\varphi \tag{6.14}$$

Using (6.13), the CPF (the red area in Fig. 6.8) obtained as

$$CPF = -\frac{V_o V_{uc}}{8\pi n\omega L_t}\varphi^2 \tag{6.15}$$

Obviously, the CPF is zero when $\varphi = 0$. This fact is shown in Fig. 6.9 where the circulating power CPF (red line) with the average power P_{uc} (blue line) are plotted against φ for different angles.

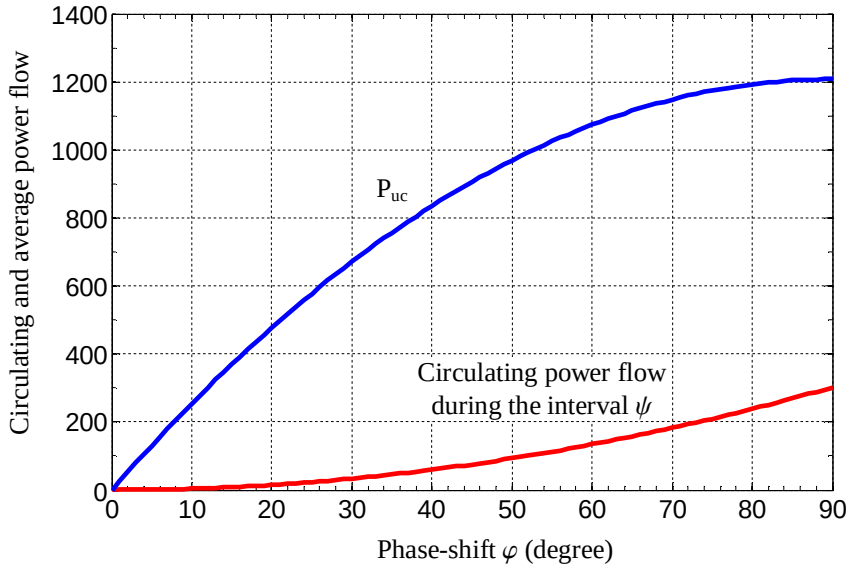


Fig. 6.9 Averaging power flow (blue line) and circulating power flow of the BDC operating under the CPC with $2nV_{uc}=V_o$ and UCDM.

It can be seen that the CPF increases as the phase-shift increases. This means that as the phase-shift is increased in respect to the required output power more circulating energy is freewheeling through the anti-parallel diodes of the MOSFET's and flows back to the input source. Due to the high reverse-recovery charge Q_{rev} of MOSFETs anti-parallel diodes[5] this energy leads to an increase in reverse-recovery losses[6] as well as conduction losses of the MOSFETs.

Hence, when the BDC is operating with CPC modulation, CPF can be reduced either by minimizing L_t (with a higher RMS current rating as a consequence) or by selecting a smaller phase-shift φ (at the detriment of the power transfer capability of BDC).

Therefore, an alternative modulation is required to minimize the CPF interval without these unwanted effects.

[5] Reverse-recovery charge Q_{rev} for the anti-parallel diode of the bridge MOSFET is 5µC compared to the 28nC for the Schottkey diodes used in the voltage-doubler.
[6] As indicated in Section 3.3.1.3, the reverse-recovery losses change in relation to the Q_{rev}

6.3.2 Determination of CPF Interval

For the interval T_1+T_2 in Fig. 6.2e, the primary current $i_{Lt}(\theta)$ is given by:

$$i_{Lt}(\theta) = \frac{V_o + 2nV_{uc}}{2n\omega L_t}\theta + I_{to} \tag{6.16}$$

for operation in UCDM at $2nV_{uc} > V_o$.

According to Table 6.1 I_{to} is given by:

$$I_{to} = \frac{V_o(\pi - 2\varphi_1) - 2nV_{uc}\varphi_2}{4n\omega L_t} \tag{6.17}$$

As can be seen in Fig. 6.2e, during the CPF interval (i.e. Interval T_1) the current through the inductance L_t ramps from a value of I_{to} until it reaches zero at $\theta = \psi$. By substituting (6.17) into (6.16) the value of $i_{Lt}(\theta)$ at $\theta = \psi$ can be expressed as:

$$I_{\psi} = \frac{V_o(\pi + 2\psi - 2\varphi_1) + 2nV_{uc}(2\psi - \varphi_2)}{4n\omega L_t} \tag{6.18}$$

where I_{ψ} is equal zero for all $I_{to} \leq 0$

The duration of the CPF interval is therefore equal to:

$$\psi = \frac{2nV_{uc}\varphi_2 - V_o(\pi - 2\varphi_1)}{2(V_o + 2nV_{uc})} \tag{6.19}$$

Similarly, for the BDC operating in UCCM (where φ_1 and $\varphi_2 < 0$) the CPF interval is obtained as:

$$\psi = \frac{2nV_{uc}\varphi_2 + V_o(\pi + 2\varphi_1)}{2(V_o + 2nV_{uc})} \tag{6.20}$$

According to Table 5.1 and (5.3) the CPF interval for the CPC modulation (i.e. $\varphi_2 = \pi$ and $\varphi_1 = \varphi$) can be obtained as:

$$\psi = \frac{2n\pi V_{uc} - V_o(\pi - 2\varphi)}{2(V_o + 2nV_{uc})} \tag{6.21}$$

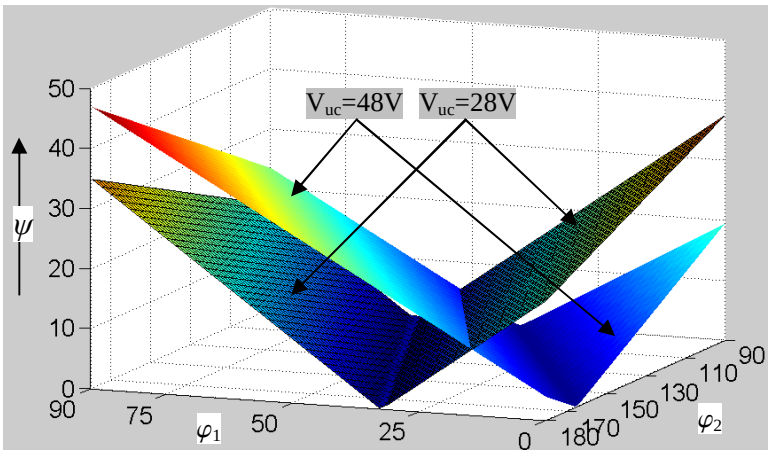


Fig. 6.10 CPF interval durations against $\varphi 1$ and $\varphi 2$ for UCDM

In Fig. 6.10 the contour surface of the CPF interval in relation to φ_1 and φ_2 is depicted for two different UC voltage (V_{uc} = 48V and 28V) when $0 \le \varphi_1 \le 0.5\pi$, $0.5\pi \le \varphi_2 \le \pi$, and $P_{uc} > 0$. It can be seen that for certain combinations of φ_1 and φ_2 a zero CPF interval can be obtained. In contrast, for CPC a zero CPF interval can only be realised for one operating phase-shift angle, which is

$$\varphi = \frac{\pi(V_o - 2nV_{uc})}{2V_o} \tag{6.22}$$

Hence, in general minimising the CPF interval is not possible for CPC.

6.3.3 Impact of the CPF Interval on the Converter Parameters

An expression that relates the average power P_{uc} explicitly to the CPF interval ψ can be

derived as follows:

According to the current waveform for Mode V in Fig. 6.2e, the transferred power can be expressed as

$$P_{uc} = \frac{V_{uc}}{\pi}\left(\frac{1}{2}(I_{to})\psi + \frac{1}{2}(I_{\varphi_1} + I_{\psi})(\varphi_1 - \psi) + \frac{1}{2}(I_{\varphi_1} + I_{\varphi_2})(\varphi_2 - \varphi_1)\right) \quad (6.23)$$

Substituting (6.18) and the values of the currents I_{to}, $I_{\varphi 1}$, I_{ψ}, and $I_{\varphi 2}$ at the commutation instants 0, φ_1, ψ, and φ_2 from Table 6.1 (Mode V) into (6.23), the transferred power is obtained as

$$P_{uc} = \frac{V_{uc}}{8n\pi\omega L_t}\{V_{uc}[2n\varphi_1\varphi_2 - 4n\psi\varphi_1] + V_o[2\pi\varphi_2 - \pi\varphi_1 - 2\psi\varphi_1 - 2\varphi_1^2 + 4\varphi_1\varphi_2 - 2\varphi_2^2]\} \quad (6.24)$$

As can be seen the variable ψ is introduced in the power equation of the BDC.

It is seen from the new definition of power flow in (6.24) that the CPF interval has a considerable impact on the average power transfer of the BDC. This can be observed more clearly in Fig. 6.11, where is P_{uc} plotted against φ_1 and φ_2 for different values of ψ. A larger CPF interval the power capability of the converter is reduced.

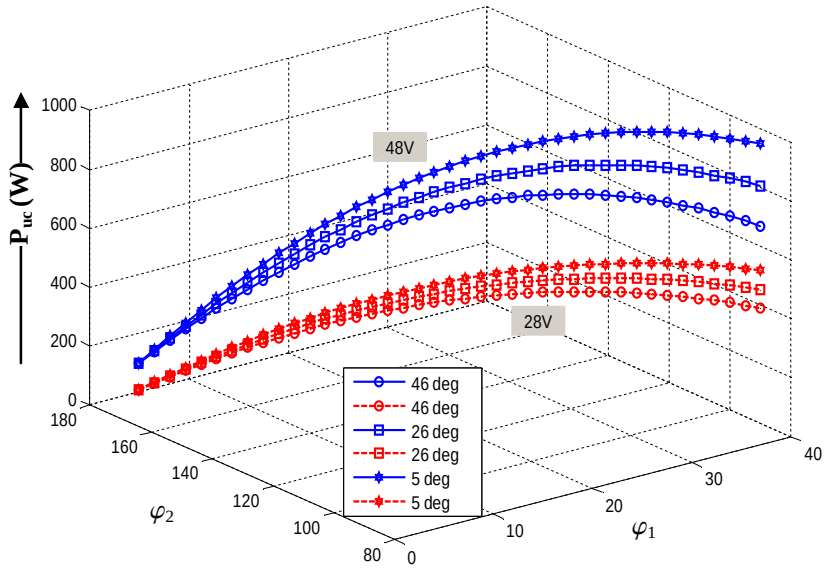


Fig. 6.11 Output power capability of BDC for different angles ψ

As shown in Fig. 6.10, the maximum CPF interval is 46^0 at $\varphi_1 = 90^0$ and $\varphi_2 = 180^0$ when V_{uc} = 48V. Also, it is worth mentioning that the CPF interval ψ is not a controllable parameter such as the phase-shift φ_1 and φ_2 but it is an interval implicit in the operation of the BDC and its parameters:

$$\psi = f(\varphi_1, \varphi_2, V_{uc}, V_o) \qquad (6.25)^7$$

The relation between the CPF interval and the primary RMS current can be obtained as follows:

From (6.24) the expression that determines the series inductance value can be derived as:

$$L_t = \frac{V_{uc}}{8n\pi\omega P_{uc}}(V_o[-\pi\varphi_1 - 2\psi\varphi_1 - 2\varphi_1^2 + 2\pi\varphi_2 + 4\varphi_1\varphi_2 - 2\varphi_2^2] + V_{uc}[-4n\psi\varphi_1 + 2n\varphi_1\varphi_2]) \qquad (6.26)$$

After substituting (6.26) in (6.6) the RMS current through the primary can be derived

[7] See (6.19) and (6.20)

as:

$$I_{rms} = \frac{1}{\sqrt{2\pi}}\left[\sqrt{\frac{4\pi^2 P_{uc}^2 b}{3V_{uc}^2(V_o+2nV_{uc})a}} + \sqrt{\frac{4\pi^2 P_{uc}^2((\pi V_o+2nV_{uc}(2\varphi_1-\varphi_2))^3-c)}{3V_{uc}^2(V_o-2nV_{uc})a}} + \sqrt{\frac{4\pi^2 P_{uc}^2((V_o(\pi-2\varphi_1)-2nV_{uc}\varphi_2)^3+c)}{3V_o V_{uc}^2 a}}\right] \tag{6.27}$$

with

$$a = [\pi V_o\varphi_1 + 2\psi V_o\varphi_1 + 4n\psi V_{uc}\varphi_1 + 2V_o\varphi_1^2 - 2\pi V_o\varphi_2 - 4V_o\varphi_1\varphi_2 - 2nV_{uc}\varphi_1\varphi_2 + 2V_o\varphi_2^2]^2$$

$$b = \{[\pi V_o + 2nV_{uc}(2\varphi_1 - \varphi_2)]^3 - [V_o(\pi - 2\varphi_1) - 2nV_{uc}\varphi_2]^3\} \tag{6.28}$$

and

$$c = [V_o(\pi + 2\varphi_1 - 2\varphi_2) + 2nV_{uc}\varphi_2]^3$$

where the CPF interval ψ is explicit.

In Fig. 6.12 the RMS values of the primary winding currents are shown against φ_1 and φ_2 for different durations of ψ. It can be seen that in all cases a shorter duration of ψ results in a lower minimum RMS current at the same voltage and power levels.

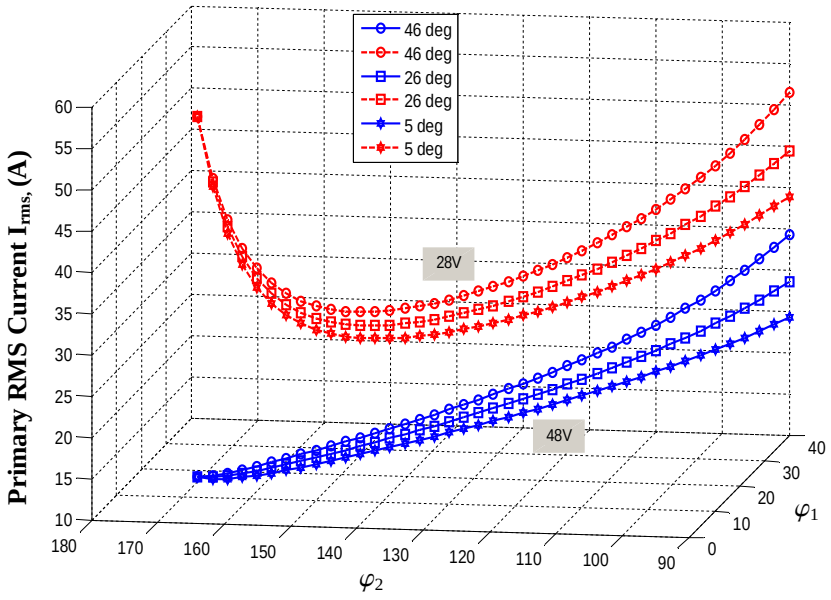


Fig. 6.12 Primary RMS current for different duration of CPF intervals for P_{uc} = 600W

Based on the above analysis, it can be concluded that a longer CPF interval (i.e. more circulating energy through the converter's switches) does not only increase the RMS current (and thus the conduction losses as a consequence) but also reduces the power capability of the BDC at a certain power operation range. Hence, it is desirable to eliminate this interval or minimise it, as proposed in the next section.

6.4 Operation Principle of the Optimal Modulation Scheme

According to Section 6.3.2, finding the angles φ_1 and φ_2 in Fig. 6.10 that realize a zero-CPF interval assists to develop a modulation scheme leading the BDC to operate with minimum losses and a higher efficiency as will be described next. However, the zero-CPF interval is limited by the required power transfer and the UC voltage variations. In order for the BDC to operate over the full power range with minimum CPF, RMS current, and peak current, two more operational modes have been developed (see Sections 6.4.2 and 6.4.3).

Again, ultracapacitor charging mode UCCM denotes a power transfer from the DC link to the ultracapacitor energy buffer (negative power $P_{uc} < 0$ and $\varphi < 0^0$) and UCDM denotes a power transfer from the ultracapacitor energy buffer to the DC link (positive power $P_{uc} > 0$ and $\varphi > 0^0$).

6.4.1 Zero CPF Interval Mode

From Fig. 6.10, and equation (6.19) it is evident that for constant V_o the CPF interval depends on φ_1 and φ_2, the UC voltage variation, the transformer turns ratio and the required power. Hence, the phase-shift angles φ_1 and φ_2 must be calculated in relation to the UC voltage and the required power to ensure operation at zero CPF. This mode is called the zero–CPF interval (ZCPF) mode.

According to (6.19), to realize a zero-CPF interval (i.e. $\psi = 0$) the phase-shift angle φ_2 must be equal to:

$$\varphi_2 = \frac{V_o(\pi - 2\varphi_1)}{2nV_{uc}} \tag{6.29}$$

when the BDC is in UCDM[8] and $2nV_{uc} > V_o$.

Substitution of (6.29) in the average power equation (6.9) shows that the required phase-shift angle φ_1 in ZCPF mode is given by:

$$\varphi_1 = \frac{\pi V_o^3 - n\pi V_o^2 V_{uc}}{2V_o^3} - \frac{\sqrt{-16\pi\omega L_t n^3 P_{uc} V_o^3 V_{uc} + n^2\pi^2 V_o^4 V_{uc}^2}}{2V_o^3} \tag{6.30}$$

[8] For $2nV_{uc} = V_o$, the phase-shift φ_2 only changes in relation to φ_1. Thus, $\varphi_2 = \pi - 2\varphi_1$.

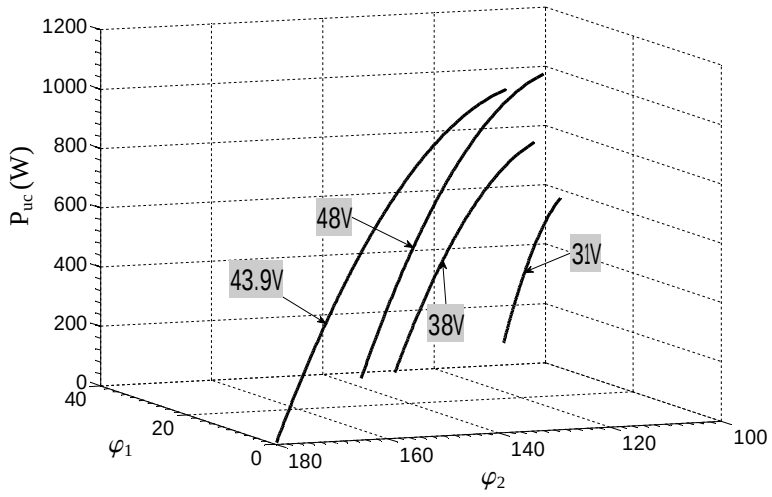


Fig. 6.13 Phase-shift angles required to achieve zero-CPF for the UCDM

Using (6.29) and (6.30) the required combinations of φ_1 and φ_2 that achieve zero-CPF interval can be plotted against the transferred power P_{uc} for the different UC voltages as shown in Fig. 6.13. The achievable power range for ZCPF mode lies within the power transfer range of the BDC shown in Fig. 6.6. However, the power achieved by the BDC in the ZCPF mode is lower than the power capability of the BDC in Mode V (see Section 6.2.1.2). Thus, to find the boundaries of the ZCPF mode the operation of the BDC in this mode has been analysed for low and high power operations.

The theoretical waveforms and equivalent circuits of the operation of the BDC under low and high power transfer when $2nV_{uc} > V_o$ and $P_{uc} > 0$ (i.e. UCDM) are shown in Fig. 6.14 to Fig. 6.17 respectively. A brief description of each mode of operation is given below.

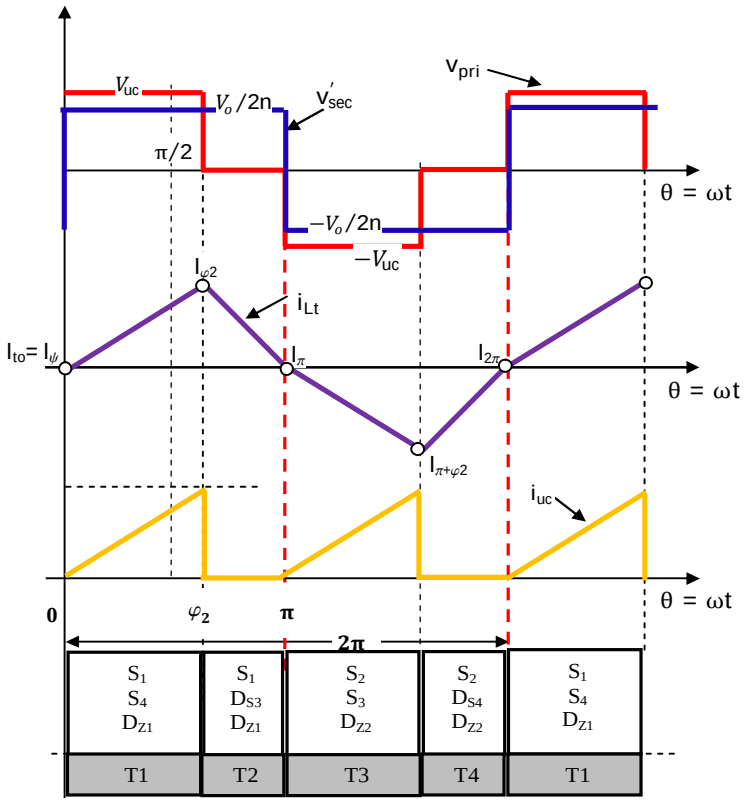


Fig. 6.14 Key waveforms of the BDC operating in ZCPF mode for low power transfer in UCDM when $2nV_{uc}>V_o$

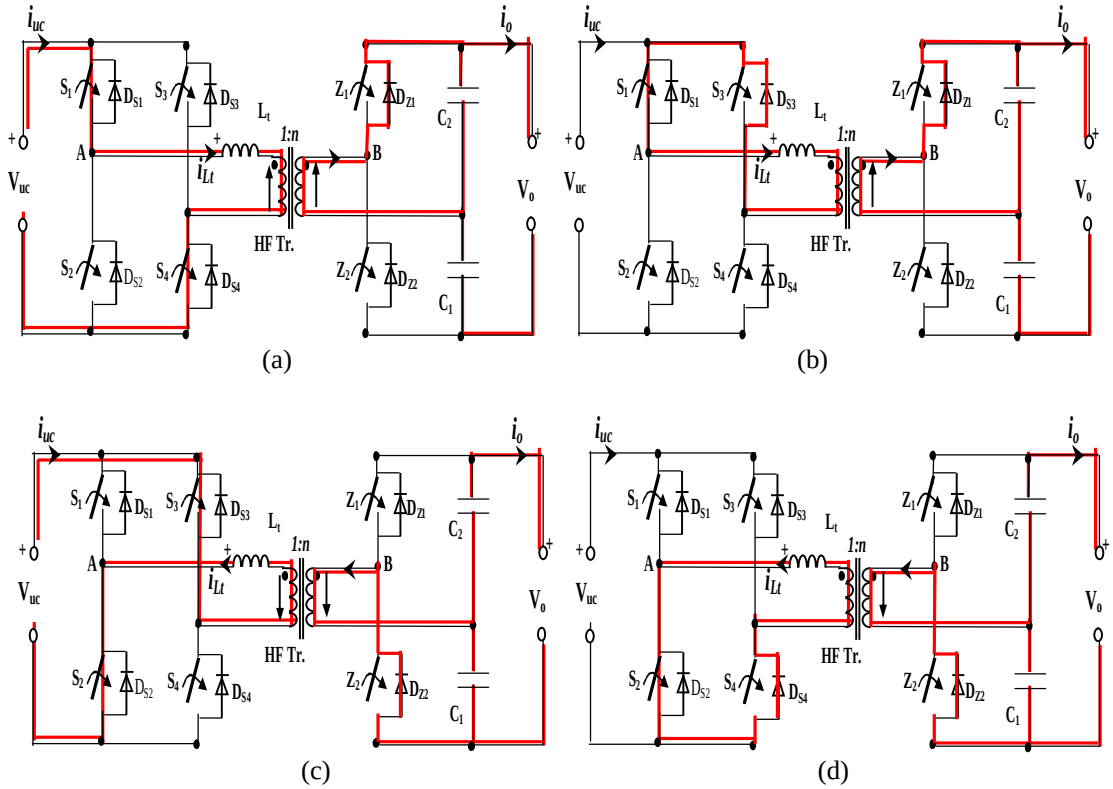


Fig. 6.15 Detailed equivalent circuits of the BDC for each operating state under ZCPF mode for low power transfer in UCDM: (a)T_1: ($0 \le \theta \le \varphi_2$), (b)$T_2$: ($\varphi_2 \le \theta \le \pi$), (c) T_3: ($\pi \le \theta \le \pi+\varphi_2$), (d) T_4: ($\pi+\varphi_2 \le \theta \le 2\pi$)

A- Low Power Operation

It can be seen from Fig. 6.13 that for low power transfer the phase-shift φ_1 is very small and reaches 0^0 at the minimum achievable power during ZCPF mode. Therefore, for low power transfer only the inner phase-shift φ_2 controls the power flow of the BDC. Fig. 6.14 shows the waveforms of the primary voltage $v_{pri}(t)$, the secondary voltage referred to the primary $v'_{sec}(t)$, the primary current, and the input current during ZCPF mode at low power. The equivalent circuit for each mode during one-cycle (i.e. T_1-T_4) is given in Fig. 6.15a-d.

Mode T_1 ($0 \le \theta \le \varphi_2$): Before this mode current is circulating through the primary winding and the output voltage is maintained by C_1 and C_2. At $\theta = 0$ switch S_1 is turned on with ZCS (since $I_{to} = 0$) while the switch S_2 is turned off with hard switching. Since $\varphi_1 = 0$ there is no phase-shift between $v_{pri}(t)$ and $v'_{sec}(t)$ and the anti-parallel diode D_{z1} turns on with zero current. At $\theta = \varphi_2$ switch S_4 can be gated off with zero volt since $I_{\varphi 2} > 0$ (see (6.4))[9]. As shown in Fig. 6.15a, during this mode power is delivered to the DC link side and thus the primary current $i_{Lt}(\theta)$ starts to increase from $I_{to} = 0$ according to

$$i_{Lt}(\theta) = \frac{2nV_{uc} - V_o}{2n\omega L_t}\theta \qquad (6.31)$$

Mode T_2 ($\varphi_2 \le \theta \le \pi$): At $\theta = \varphi_2$ the parasitic capacitance of S_3 will be discharged by $I_{\varphi 2}$, and the anti-parallel diode D_{S3} start conducting. Hence, S_3 can be turned on with ZVS. As S_1 remains on until π, the primary side of the transformer is shorted through S_1 and D_{S3} and the inductor current circulates through the primary winding, as shown in Fig. 6.15b. During this mode the transferred instantaneous power $P_{uc}(t)$ is equal to zero and the primary current $i_{Lt}(\theta)$ falls to zero at $\theta = \pi$ with a slope equal to

[9] ZVS is maintained by control of the amount of current in $i_{Lt}(\theta)$ at the switching instant.

$$i_{Lt}(\theta) = \frac{-V_o}{2n\omega L_t}(\theta - \varphi_2) + I_{\varphi_2} \tag{6.32}$$

where $I_{\varphi 2}$ can be obtained from (6.31) as

$$I_{\varphi_2} = \frac{2nV_{uc} - V_o}{2n\omega L_t}\varphi_2 \tag{6.33}$$

The operation modes T_3 and T_4 during the next half-cycle are complementary to the modes T_1 and T_2, as shown in Fig. 6.15 c and d.

From the BDC operation in Fig. 6.15 and the primary current and voltage waveforms in Fig. 6.14, the transferable power $P^{b}_{uc\_ZCPF\_L}$ which can be achieved during ZCPF for the low power operation is obtained as:

$$P^{b}_{uc\_ZCPF\_L} = \frac{V_{uc}}{2\pi} I_{\varphi_2}\varphi_2 = \frac{V_{uc}(V_{uc} - \frac{V_o}{2n})\varphi_2^2}{2\pi\omega L_t} \tag{6.34}$$

where $I_{\varphi 2}$ is defined in (6.33).

It can be seen from (6.34), that during low power operation the power transfer is solely controlled by φ_2 in this mode. In order to achieve I_{to} and I_{π} equal 0:

$$(V_{uc} - \frac{V_o}{2n})\varphi_2 = \frac{V_o}{2n}(\pi - \varphi_2) \tag{6.35}$$

Hence, the minimum phase-shift angles of φ_1 and φ_2 can be obtained as.

$$\varphi_{1\_ZCPF}^{min,b} = 0 \text{ and } \varphi_{2_{ZCPF}}^{min,b} = \pi V_o/2nV_{uc} \tag{6.35a}$$

Based on the condition in (6.35), the minimum transferable power ($P_{uc\_ZCPF}^{min,b}$) in this mode of operation is equal to:

$$P_{uc\_ZCPF}^{min,b} = \frac{\pi V_o^2 (V_{uc} - \frac{V_o}{2n})}{8n^2 \omega L_t V_{uc}} \tag{6.36}$$

Using a similar procedure the minimum phase-shift angles of φ_1 and φ_2 when $2nV_{uc} < V_o$ and $P_{uc} > 0$ can be determined and the results are shown in Table 6.3.

TABLE 6.3
ZCPF INTERVAL MODE BOUNDARY WHEN $2nV_{UC} < V_O$ AND $P_{UC} > 0$ FOR LOW POWER OPERATION

$P_{uc\_ZCPF\_L}^{c} = \frac{V_o V_{uc}(2\pi\varphi_1 - 2\varphi_1^2)}{4n\pi\omega L_t}$	$P_{uc\_ZCPF}^{min,c} = \frac{\pi V_{uc}(V_o^2 - 4n^2 V_{uc}^2)}{8n\omega L_t V_o}$
$\varphi_{1\_ZCPF}^{min,c} \cong \frac{\pi(V_o - 2nV_{uc})}{2V_o}$	$\varphi_{2_{ZCPF}}^{min,c} = \pi$

In order to assess the performance of the BDC with the new optimal modulation, the primary RMS current has been derived for each mode, as described below and in the next Sections 6.4.2 and 6.4.3.

According to (5.9) and the primary current waveform in Fig. 6.14, the primary RMS current is obtained as:

$$I_{rms} = \left[\frac{1}{2\pi}\left\{\int_0^{\varphi_2}\left(\frac{2nV_{uc}-V_o}{2n\omega L_t}\theta\right)^2 d\theta + \int_{\varphi_2}^{\pi}\left(\frac{-V_o}{2n\omega L_t}(\theta-\varphi_2) + I_{\varphi_2}\right)^2 d\theta + \int_{\pi}^{\pi+\varphi_2}\left(-\left[\frac{2nV_{uc}-V_o}{2n\omega L_t}(\theta-\pi)\right]\right)^2 d\theta + \int_{\pi+\varphi_2}^{2\pi}\left(-\left[\frac{-V_o}{2n\omega L_t}(\theta-\pi-\varphi_2) + I_{\varphi_2}\right]\right)^2 d\theta\right\}\right]^{\frac{1}{2}} \tag{6.37}$$

Substituting (6.33) in (6.37) and solving the integrals in (6.37), the RMS current obtained as

$$I_{rms} = \frac{1}{2\sqrt{3\pi}n\omega L_t}\left[\sqrt{\pi^3}V_o + 2nV_{uc}\sqrt{(3\pi - 2\varphi_2)}\varphi_2 + \sqrt{2nV_oV_{uc}\varphi_2(-3\pi^2 + \varphi_2^2)}\right] \quad (6.38)$$

Substituting L_t from (6.34) in (6.38) the primary RMS current in respect to the average power P_{uc} is derived as:

$$I_{rms} = 2\sqrt{\frac{\pi}{3}}\sqrt{\frac{P_{uc}^2(\pi^3V_o^2 + 4n^2V_{uc}^2(3\pi - 2\varphi_2)\varphi_2^2 + 2nV_oV_{uc}\varphi_2(-3\pi^2 + \varphi_2^2))}{V_{uc}^2(V_o - 2\,nV_{uc})^2\varphi_2^4}} \quad (6.39)$$

B- High Power Operation

As the required power increases both φ_1 and φ_2 have to be recalculated as shown in Fig. 6.13 in order to maintain operation at ZCPF. Hence, the BDC is controlled by two phase-shift angles. Similar to low power operation, in ZCPF mode I_{to} is maintained equal to zero over the full range of this mode to maintain the lowest CPF interval and realise ZCS for the leading leg of the bridge.

Fig. 6.16 shows the waveforms of the primary voltage $v_{pri}(t)$, the secondary voltage referred to the primary $v'_{sec}(t)$, the primary current, and the input current during the ZCPF mode for high power operation. The equivalent circuit for each mode during one-cycle (i.e. T_1-T_6) is given in Fig. 6.17 a-f.

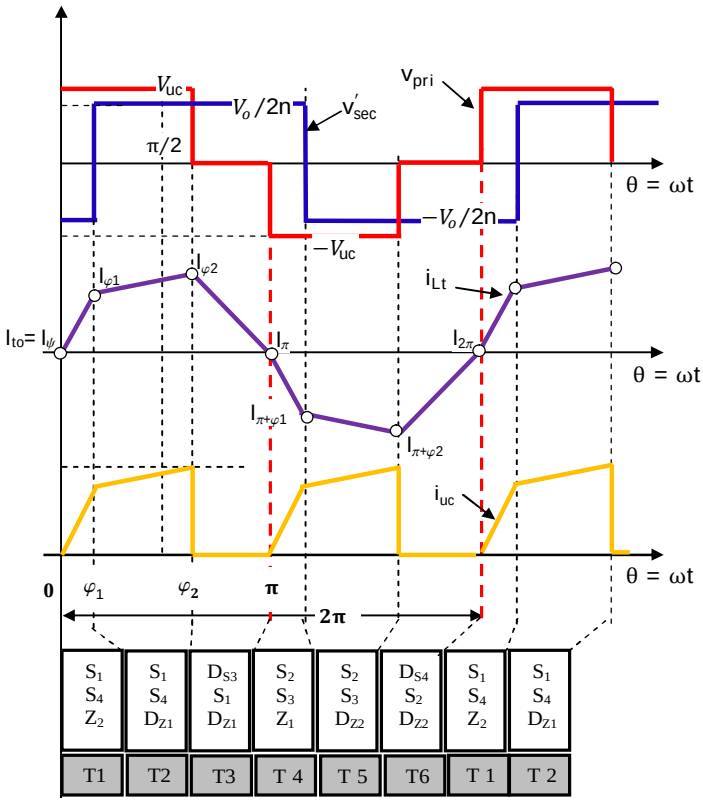


Fig. 6.16 Key waveforms of the BDC operating in ZCPF mode for high power transfer in UCDM when $2nV_{uc}>V_o$

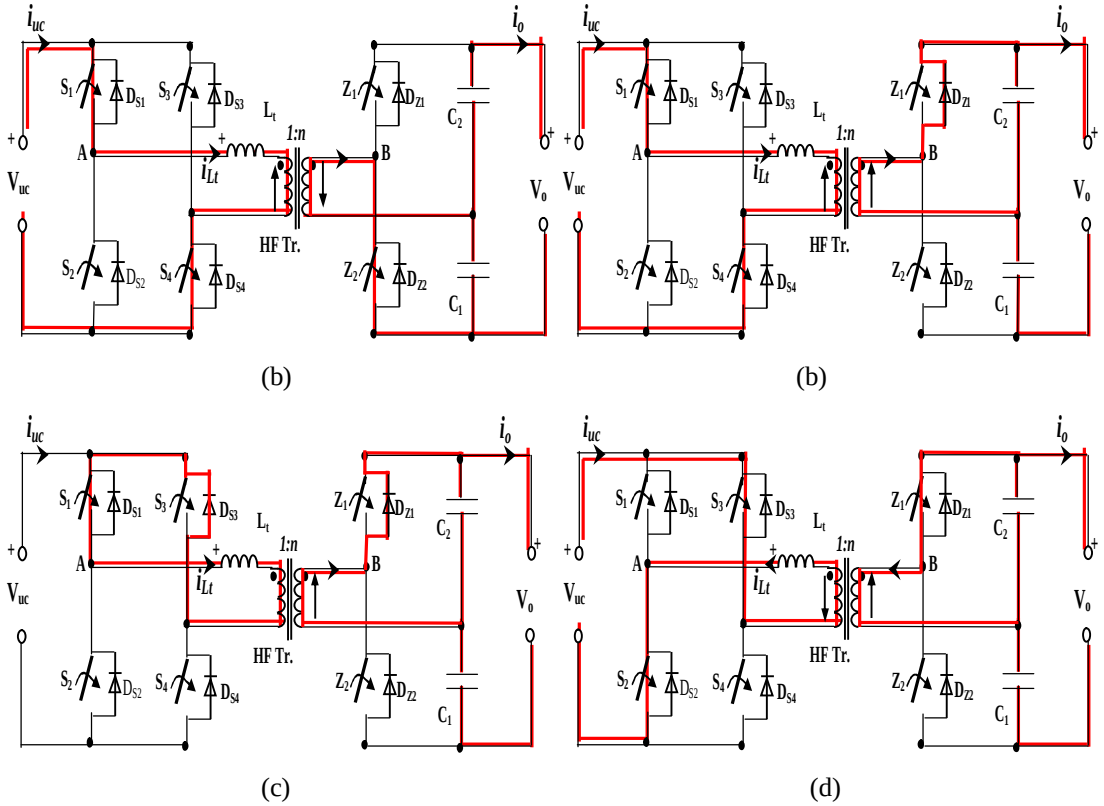


Fig. 6.17 Detailed equivalent circuits of the BDC for each operating state under ZCPF mode for high power transfer in UCDM (continued on the next page)

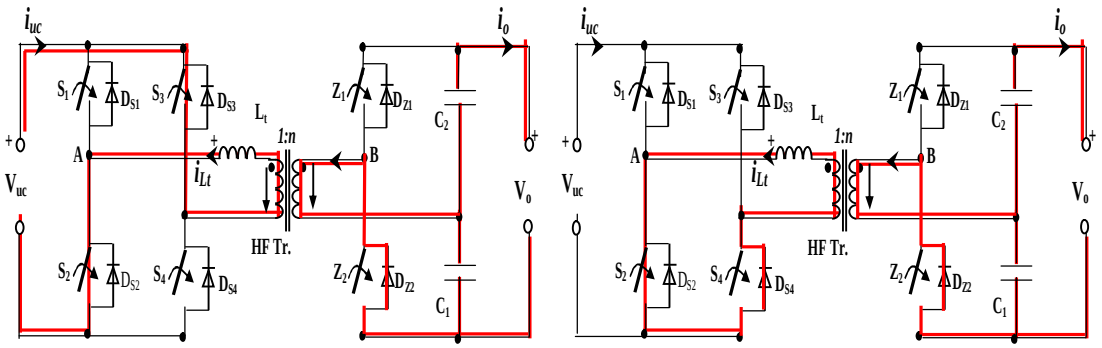


Fig. 6.17cont. Detailed equivalent circuits of the BDC for each operating state under ZCPF mode for high power transfer in UCDM (a)T_1: ($0 \le \theta \le \varphi_1$), (b)$T_2$: ($\varphi_1 \le \theta \le \varphi_2$), (c) T_3: ($\varphi_2 \le \theta \le \pi$), (d) T_4: ($\pi \le \theta \le \pi+\varphi_1$), (e) T_5: ($\pi+\varphi_1 \le \theta \le \pi+\varphi_2$), (f) T_6: ($\pi+ \varphi_2 \le \theta \le 2\pi$)

Mode T_1 ($0 \le \theta \le \varphi_1$): This mode similar to the Mode T_1 of low power transfer in respect of the SSW operation for S_1 and S_2. However, in this operating mode the switch Z_2 is conducts with ZVS at $\theta = 0^0$ since its anti-parallel diode D_{Z2} turns on prior to $\theta = 0^0$ (see Fig. 6.17a). Since $2nV_{uc} > V_o$ the primary current starts to rise until it reaches $I_{\varphi 1}$ at $\theta = \varphi_1$, where the current ramps up according to

$$i_{Lt}(\theta) = \frac{2nV_{uc}+V_o}{2n\omega L_t}\theta \qquad (6.40)$$

Mode T_2 ($\varphi_1 \le \theta \le \varphi_2$): As shown in Fig. 6.17b, the switches S_1 and S_4 are still conducting until $\theta = \varphi_2$. However, at $\theta = \varphi_1$ switch Z_1 is turned on. Due to $I_{\varphi 1} > 0$ the stored energy in L_t starts to discharge the parasitic capacitance of Z_1, leading the anti-parallel diode D_{Z1} to turn on. Therefore, Z_1 can be turned on with ZVS at Mode T_4 (see Fig. 6.17d). During this mode the primary current still increases, where the slope of the current rise is given by:

$$i_{Lt}(\theta) = \frac{2nV_{uc}-V_o}{2n\omega L_t}(\theta - \varphi_1) + I_{\varphi_1} \qquad (6.41)$$

During Modes T_1 and T_2 the power is delivered to the output through the series inductance L_t.

Mode T_3 ($\varphi_2 \leq \theta \leq \pi$): During this mode the switches S_1 and S_3 are overlapping until $\theta = \pi$ as shown in Fig. 6.17c. Thus, the input current is circulating through the primary winding and decreases according to

$$i_{Lt}(\theta) = \frac{-V_o}{2n\omega L_t}(\theta - \varphi_2) + I_{\varphi_2} \tag{6.42}$$

The BDC operations during Modes T_4-T_6 are similar to Modes T_1-T_3.

By substituting $\theta = \varphi_1$ in (6.40) the value of the current $I_{\varphi 1}$ is obtained as:

$$I_{\varphi 1} = \frac{2nV_{uc} + V_o}{2n\omega L_t}\varphi_1 \tag{6.43}$$

Substituting $\theta = \varphi_2$ and (6.43) into (6.41) the value of the current $I_{\varphi 2}$ is derived as:

$$I_{\varphi 2} = \frac{V_o(2\varphi_1 - \varphi_2) + 2nV_{uc}\varphi_2}{2n\omega L_t} \tag{6.44}$$

Based on the BDC operation in Fig. 6.17 and using (6.43) and (6.44), the power that can be transferred during ZCPF mode for high power operation is given by:

$$P^{b}_{uc_{ZCPF_H}} = \frac{V_{uc}\left(2nV_{uc}\varphi_2^2 - V_o(2\varphi_1^2 - 4\varphi_1\varphi_2 + \varphi_2^2)\right)}{4\pi n\omega L_t} \tag{6.45}$$

Substituting (6.29) in (6.45) and equating $(\partial P^{b}_{uc\_ZCPF\_H}/\partial\varphi_1)$ to zero, the maximum phase-shift angle of φ_1 during ZCPF mode is obtained as:

$$\varphi^{max,b}_{1\_ZCPF} = \frac{\pi V_o^2}{2(V_o^2 + 2nV_oV_{uc} + 2n^2V_{uc}^2)} \tag{6.46}$$

Substitution of (6.46) in (6.29) gives the maximum phase-shift angle of φ_2 during ZCPF mode as

$$\varphi_{2\_ZCPF}^{max,b} = \frac{\pi V_o(V_o + nV_{uc})}{V_o^2 + 2nV_oV_{uc} + 2n^2V_{uc}^2} \tag{6.47}$$

Substituting $\varphi_{1\_ZCPF}^{max,b}$ and $\varphi_{2\_ZCPF}^{max,b}$ into (6.45), the maximum power transfer of the BDC at high power operation under ZCPF is given by:

$$P_{uc\_ZCPF}^{max,b} = \frac{\pi V_o^2 V_{uc}(V_o + 2nV_{uc})}{8n\omega L_t(V_o^2 + 2nV_oV_{uc} + 2n^2V_{uc}^2)} \tag{6.48}$$

Using a similar procedure the boundaries of ZCPF interval mode for UCCM can be obtained.

According to (5.9) and the waveform of the primary current in Fig. 6.16, the primary RMS current in respect to the average power P_{uc} is found as:

$$\begin{aligned} I_{rms} &= \frac{2\sqrt{\frac{\pi}{3}}P_{uc}}{V_{uc}(-2nV_{uc}\varphi_2^2 + V_o(2\varphi_1^2 - 4\varphi_1\varphi_2 + \varphi_2^2))}\left\{\sqrt{V_o^2(\pi^3 - 6\pi^2\varphi_1 + 12\pi\varphi_1^2 - 6\varphi_1^3)}\right. \\ &+ \sqrt{4n^2V_{sc}^2(3\pi - 2\varphi_2)\varphi_2^2} \\ &\left. - \sqrt{2nV_oV_{uc}(2\varphi_1^3 + 3\pi^2\varphi_2 - \varphi_2^3 + 6\varphi_1\varphi_2(-2\pi + \varphi_2))}\right\} \end{aligned} \tag{6.49}$$

It has been shown in the preceding sections that the operation of the BDC under ZCPF mode is only possible over a limited power range. Additional modulation schemes are therefore required to allow for optimum operation of the BDC over the entire power range with minimum CPF interval and losses.

6.4.2 Inner Single Phase-Shift Mode

Another mode has been developed by setting $\varphi_1 = 0$ and modifying φ_2 only, in order for the BDC to deliver a power below that of the ZCPF interval mode. This mode has been called inner single-phase shift (ISP) mode as the power is controlled by φ_2 only. Fig. 6.18 shows the converter waveforms in this mode and the conduction status for each operating mode.

Reduction in converter efficiency is not only caused by conduction losses, but also by switching losses. The proposed ISPM introduces a small CPF interval as shown in Fig. 6.18, which is needed to achieve ZVS for the UC side switches at light load operation. Hence, S_1~S_4 are gated on with ZVS (since $I_{to} < 0$) [10]. Unlike in ZCPF mode, the switch Z_1 and Z_2 are turned on with ZCS as shown in Fig. 6.18 (Mode T_1 and T_4 respectively).

The equivalent circuits for the BDC when operating in ISP mode for UCDM corresponding to Modes T_1 to T_6, are shown in Fig. 6.19.

[10] It can be seen that the primary current $i_{Lt}(\theta)$ increases from I_{to} to $I_{\varphi 2}$ at $\theta = \varphi_2$ and reduces to I_π when $\theta = \pi$.

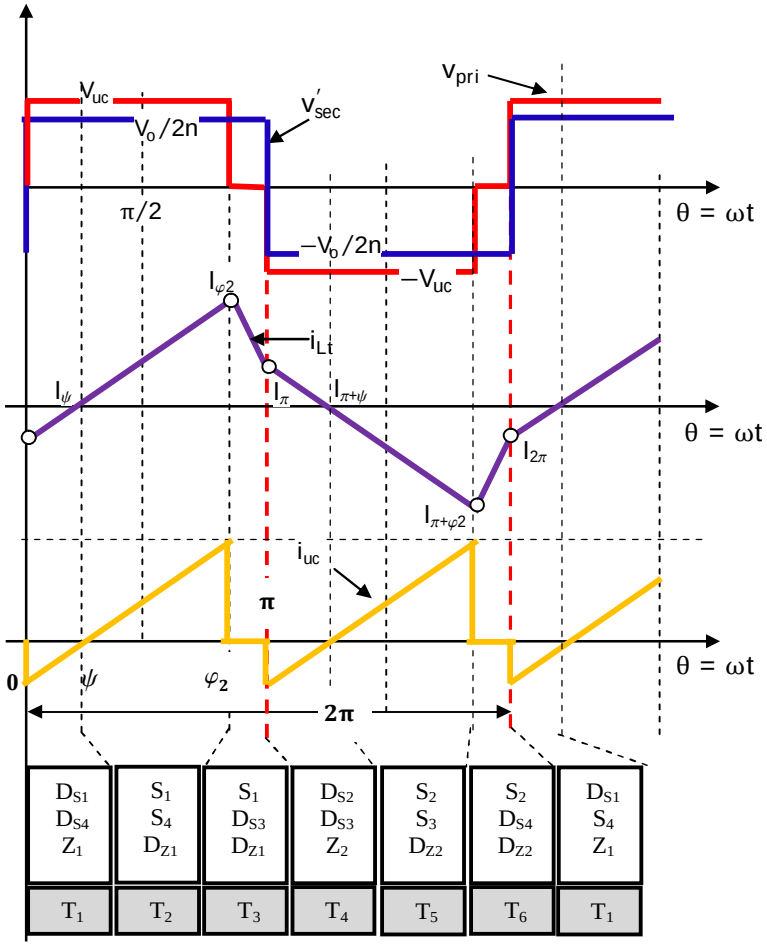


Fig. 6.18 Key waveforms of the BDC operating in ISP mode for low power transfer in UCDM when $2nV_{uc}>V_o$

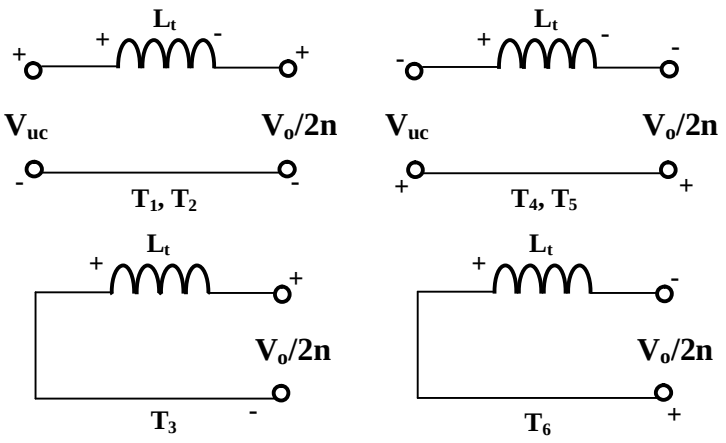


Fig. 6.19 Equivalent circuit of the BDC in ISP mode for UCDM

Based on the operation of the BDC in Fig. 6.19 and the current waveform, the values of the currents I_{to} and $I_{\varphi 2}$ are obtained as[11]

$$I_{to} = \frac{\pi V_o - 2nV_{uc}\varphi_2}{4n\omega L_t} \tag{6.50}$$

and

$$I_{\varphi_2} = \frac{V_o(\pi - 2\varphi_2) + 2nV_{uc}\varphi_2}{4n\omega L_t} \tag{6.51}$$

Using (6.50) and (6.51) and the triangular area calculation method, the power transfer during this mode is found as:

$$P_{uc}^{ISP} = \frac{V_o V_{uc}(\pi - \varphi_2)\varphi_2}{4n\pi\omega L_t} \tag{6.52}$$

when $2nV_{uc} > V_o$ and $P_{uc} > 0$.

From (6.52) the phase-shift angle φ_2 for given power and voltage levels is obtained as:

$$\varphi_2 = \frac{\pi V_o V_{uc} + \sqrt{\pi}\sqrt{-16\omega L_t n P_{uc}^{ISP} V_o V_{uc} + \pi V_o^2 V_{uc}^2}}{2V_o V_{uc}} \tag{6.53}$$

The ISP mode is a modified version of the TRM scheme. However, unlike the TRM scheme no change in the duty cycle with ISP mode is required and it can be operated even if $2nV_{uc} = V_o$, as indicated in (6.52). In addition, the primary current is always continuous and therefore a lower current stress is achieved (see Fig. 6.23).

It is found that ISP mode can operate with a small CPF interval until the phase-shift angle φ_2 is equal to 0.5π, where the maximum power achieved is:

[11] Note that $I_\pi = I_{to} = 0$ in the ZCPF interval mode while $I_\pi = -I_{to}$ for the ISP mode.

$$P_{uc\_ISP}^{max} = \frac{\pi V_o V_{uc}}{16 n \omega L_t} \quad (6.54)^{12}$$

However, because of the higher peak current in this mode the maximum transferred power $P_{uc\_ISP}^{max}$ and the phase-shift $\varphi_{2\_ISP}^{max}$ are limited to $P_{uc\_ZCPF}^{min,b}$ and $\phi_{2_{ZCPF}}^{min,b}$, for $P_{uc} > 0$ and $2nV_{uc} > V_o$.

Using (5.9) and the primary current waveform in Fig. 6.18, the primary RMS current can be expressed as:

$$I_{rms} = \frac{\sqrt{\frac{\pi}{3}} P_{uc}}{V_o V_{uc}(\pi - \varphi_2)\varphi_2} \sqrt{(\pi^3 V_o^2 + 4n^2 V_{uc}^2(3\pi - 2\varphi_2)\varphi_2^2 + 4nV_o V_{uc}\varphi_2^2(-3\pi + 2\varphi_2))} \quad (6.55)$$

6.4.3 Minimum CPF Interval Mode

In order for the BDC to deliver a power exceeding the ZCPF mode range with a minimum CPF interval, a third operational mode has been developed. This mode is called here the minimum CPF interval (MCPF) mode.

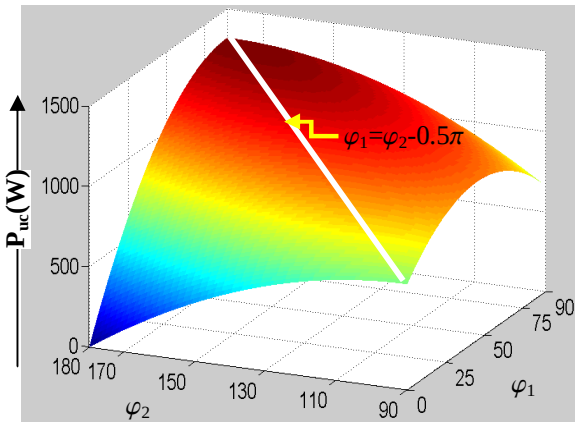


Fig. 6.20 3D contour surface of BDC power flow showing the optimum part of converter operation during high power transfer (n=7.4, L_t =10μH, V_{uc} = 48V, f_s =20kHz)

[12] By equating $(\partial P_{uc}^{ISP}/\partial\varphi_2)$ to zero the maximum phase-shift angle of $\phi_{2_{ISP}}^{max}$ is found to be $\pi/2$. After substitution of this angle in (6.52), expression (6.54) is found.

According to the contour surface of BDC power flow in Fig. 6.20[13], it can be seen that the BDC operates with a large phase-shift angle φ_1 at high power level (dark red area in the figure). As indicated in Sections 5.2 and 6.3, the operation with large phase-shift angle resulting in a longer CPF interval with a higher RMS current as a consequence. In addition, there is no closed-form expression to calculate the combination of φ_1 and φ_2 that optimises the power flow operation at the higher power level.

Therefore to achieve a minimum RMS current and to simplify the control algorithm, MCPF interval mode proposes to split the contour surface of the BDC power flow at the high power level into two parts, as indicated by the "white line" in Fig. 6.6. Hence, all the phase-shift angles at the right part (which results in reduce the power capability of the converter, see Section 6.2.1.2) and at the left part (results in a longer CPF interval, see (6.19)) of the "white line" will ignores and only the angles exactly at the "white line" will be considered. In MCPF mode a near-optimum combination can be obtained by selecting φ_1 as

$$\varphi_1 = \varphi_2 - \frac{\pi}{2} \tag{6.56}$$

During this mode the average power equation (6.9) of Mode V and the converter operating waveforms in Fig. 6.2e can be employed to find the required phase-shifts φ_1 and φ_2. Hence, by substituting (6.56) into (6.9) φ_2 can then be calculated using:

$$\varphi_2 = \frac{2\pi V_o V_{uc} - \sqrt{2\pi}\sqrt{-8Ln\omega P_{uc} V_o V_{uc} + \pi V_o^2 V_{uc}^2}}{2V_o V_{uc}} \tag{6.57}$$

The maximum power range of this mode is $P_{uc\_max}^{CPC}$ (see (5.7)), while the maximum phase-shift angles of φ_1 and φ_2 are $\pi/2$ and π, respectively.

[13] Note that this surface is plotted based on (6.9).

6.4.4 Combination of the Modulation Schemes

As detailed in Sections 6.4.1, 6.4.2, and 6.4.3 the proposed optimal modulation scheme comprises of three modulation modes as follows:

- Zero-CPF Interval Mode ZCPFM: in this mode phase-shifts φ_1 and φ_2 are changing so as to ensure a zero CPF interval
- Inner Single Phase-Shift Mode ISPM: in this mode only phase-shift φ_2 is changing and employed to deliver a power below that of the ZCPFM, where φ_1 is set to zero.
- Minimum-CPF Interval Mode MCPFM: this mode is utilised to deliver a power exceeding the ZCPFM range, and phase-shifts φ_1 and φ_2 are changing so as to ensure a minimum CPF interval.

The operation of each mode is based on the required power and the UC voltage variation. The main objective of theses modes is to find the appropriate phase-shift angles φ_1 and φ_2 that lead to the lowest value of CPF interval for the entire BDC power range. Fig. 6.21 gives an overview of the proposed optimal modulation scheme and its different operating modes (ZCPFM, ISPM, and MCPFM) for the conditions V_o = 650V, $28V \leq V_{uc} \leq 48V$,and $-1.3kW \leq P_{uc} \leq +1.3kW$, using the following parameters: n =7.4, L_t =10μH, f_s = 20kH.

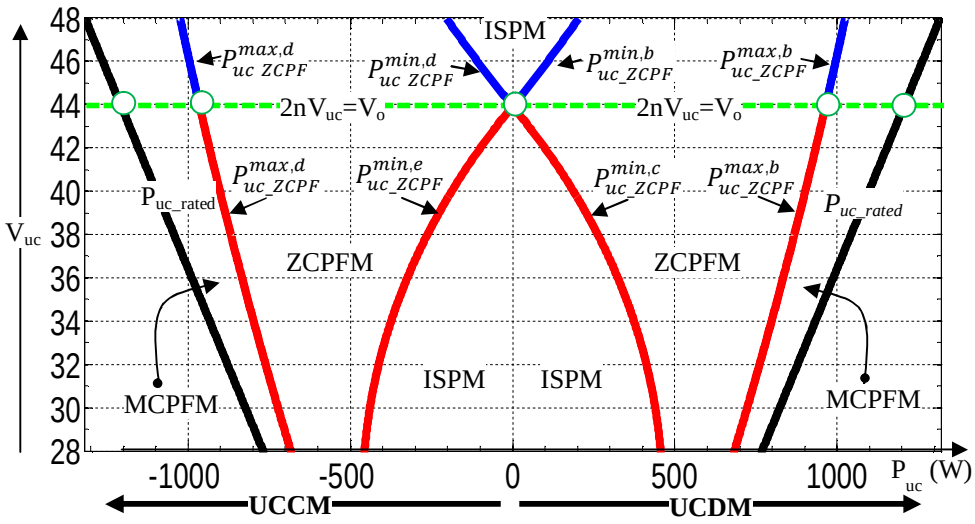


Fig. 6.21 Proposed Operating mode of the BDC for different UC voltages and different power transfer levels

As can be seen at power levels confined between the blue lines (when $2nV_{uc} > V_o$) and red lines (when $2nV_{uc} < V_o$), the operation of the BDC using the ZCPF interval mode is always possible whether for the UCCM or UCDM operation.

It is clear that the ZCPF mode range decreases with decreasing UC voltage and depends on the required power. The minimum power level of the ZCPF interval mode is achieved when $2nV_{uc} = V_o$, where $P_{uc\_ZCPF}^{min,b}$ is equal zero. To deliver a power below that of the ZCPFM, ISPM is employed which is indicated by the power levels less than $P_{uc\_ZCPF}^{min,b}$ and $P_{uc\_ZCPF}^{min,c}$ for the UCDM and $P_{uc\_ZCPF}^{min,d}$ and $P_{uc\_ZCPF}^{min,e}$ for the UCCM. At increasing power levels of the BDC, a third operational mode called MCPFM is employed. This mode is constrained by the power levels $P_{uc\_ZCPF}^{max,b}$ and P_{uc_rated} for the UCDM and $P_{uc\_ZCPF}^{max,d}$ and P_{uc_rated} for the UCCM. Consequently, the relationship between the maximum power capabilities of the optimal modulation schemes is as follows:

$$\left\{P_{uc\_ISP}^{max} < P_{uc\_ZCPF}^{max} < P_{uc\_MCPF}^{max}\right\} < P_{uc\_CPC}^{max} \tag{6.58}$$

for all $2nV_{uc} > V_o$ and $2nV_{uc} < V_o$ and

$$\left\{\left\{P_{uc\_ISP}^{max} = P_{uc\_ZCPF}^{max}\right\} < P_{uc\_MCPFM}^{max}\right\} < P_{uc\_CPC}^{max} \quad (6.59)$$

for $2nV_{uc} = V_o$.

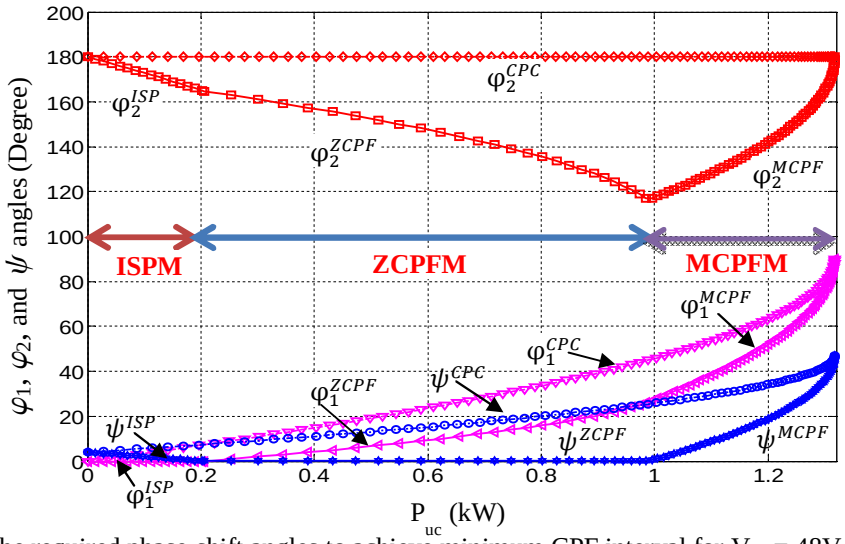


Fig. 6.22 The required phase-shift angles to achieve minimum CPF interval for V_{uc} = 48V, V_o =650V and power transfer from the UC side to the DC link side

Fig. 6.22 shows the required angles φ_1 and φ_2 to achieve minimum CPF interval over the entire power range. It can be seen that with the proposed optimal modulation the developed modes change without any discontinuities in the control parameters φ_1 and φ_2. Thus, this modulation method reduces the controller complexity[14]. In addition, compared to the CPC modulation, the proposed modulation scheme keeps the CPF interval ψ as low as possible for the full power transfer range, as illustrated in Fig. 6.22.

The calculated transformer primary RMS currents obtained with the optimal modulation scheme for each developed operating mode (ZCPFM, ISPM, and MCPFM) are shown in Fig. 6.23, where they are compared with the primary RMS currents of the BDC with

[14] Discontinuities in the phase-shift angles causes the primary current to change discontinuously and require the use of additional components in the controller to ensure a flexible mode transitions, and thus stable operation for the BDC.

CPC modulation. The phase-shift angles φ_1, φ_2 and φ for the optimal and CPC modulation that have been used to calculate the RMS current for each compared power value are listed in Table 6.4.

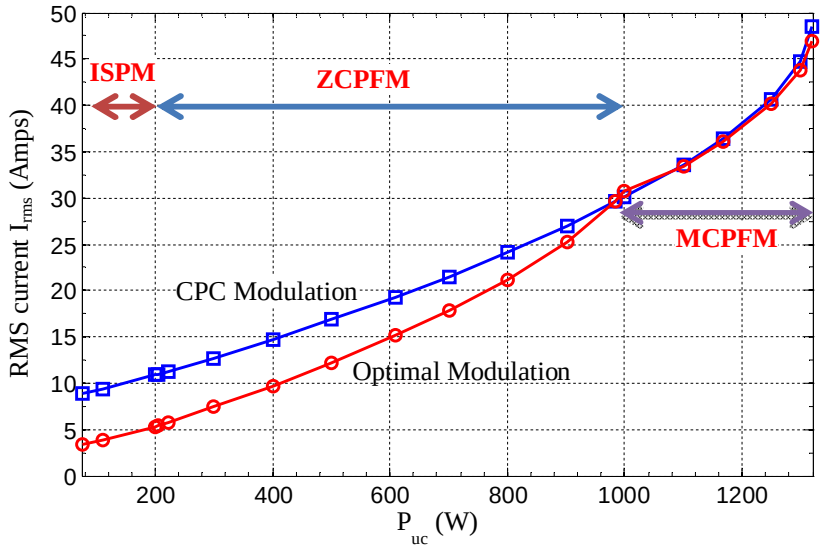


Fig. 6.23 Primary RMS currents for the optimal modulation compared to the CPC modulation method

TABLE 6.4
CERTAIN AVERAGE POWER AND PHASE-SHIFT ANGLES THAT USED TO CALCULATE THE PRIMARY RMS CURRENT FOR THE BDC OPERATES WITH OPTIMAL AND CPC MODULATION METHODS FOR UCDM

P_{UC}	OPTIMAL MODULATION		CPC MODULATION
W	φ_1 (degree)	φ_2 (degree)	φ (degree)
75	0	174.7	2.6
112	0	172	3.9
200	0	165.1	7.1
206	0	164.6	7.3
223	0.324	164.1	8
300	1.998	161	10.9
400	4.25	156.9	14.9
500	6.7	152.4	19.1
609	9.64	147.1	24
700	12.4	142	28.4
800	15.94	135.5	33.6
901	20.52	127.1	39.4
984.5	26.01	117.1	44.8
1000	27.61	114.2	45.9
1100	38.28	128.3	53.4
1167	46.97	137	59.6
1250	61.18	151.2	69.6
1300	75.3	165.3	79.7
1318	90	180	90

As shown in Fig. 6.23, at P_{uc} = 200W (when BDC under the ISPM) the primary RMS current is 5.3A, at P_{uc} = 609W the primary RMS current is 15.2A (when BDC under the ZCPFM) and at P_{uc} = 1278W the RMS current is 42.2A (when BDC under the MCPFM). Compared to the CPC modulation, the RMS current is 52%, 21% and 2% lower at 200W, 609W, and 1278W respectively. However, when the BDC is operating at the maximum power range of the ZCPF mode the RMS current at power > 1000W is slightly higher (2%) than with CPC modulation. This is due to an increase in the phase-shift angle φ_1 (see Section 6.3 about the impact of a large phase-shift on the BDC operation) and a reduced inner phase-shift φ_2 (which means a longer period for current circulating through the primary winding when the primary winding is shorted by S_1 and S_3 or S_2 and S_4), required to ensure zero CPF interval. Therefore, it is preferable to move to MCPF mode before reaching the maximum power in ZCPF mode to ensure a lower RMS current.

Fig. 6.24 shows the primary current waveforms for the three operating modes ISPM, ZCPFM, and MCPFM of the optimal modulation scheme and the current waveform between the boundaries of the modes, as derived in Sections 6.4.1, 6.4.2, and 6.4.3.

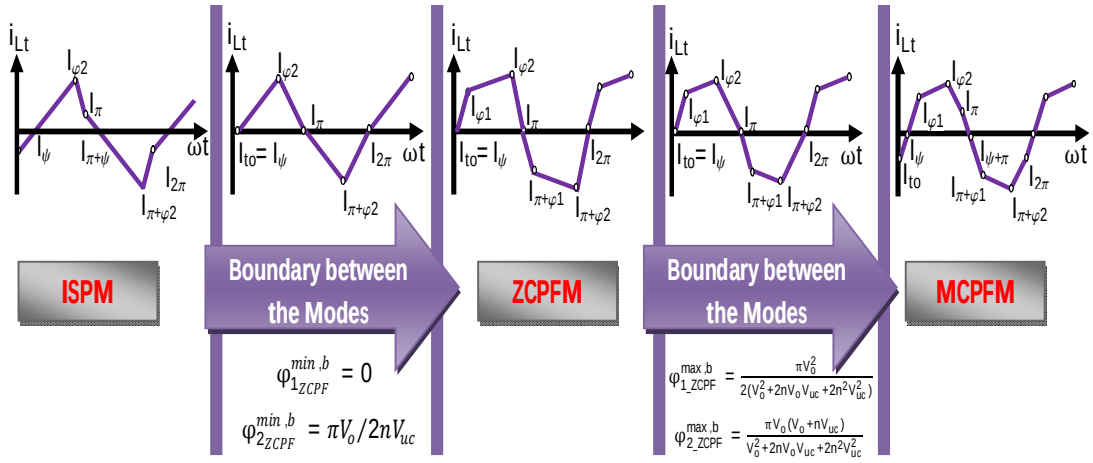


Fig. 6.24 Three modes transition of the proposed optimal modulation scheme

It can be seen in Fig. 6.24 that the optimal modulation scheme provides a seamless transition between the operating modes because the primary current $i_{Lt}(\theta)$ either ends at zero or starts from zero, as shown at the boundaries of the modes transition. As shown in the next section (see Fig. 6.40), this helps in reducing chattering between the modes.

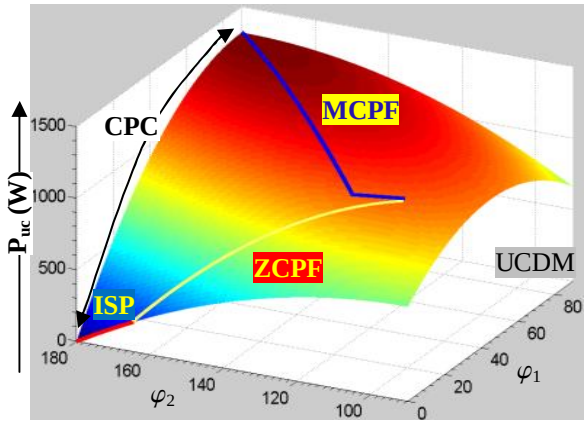


Fig. 6.25 3D contour surfaces of BDC power flow shows the trajectory of the proposed optimum modulation scheme

The relation between the power capability and the optimum phase-shift angles for each mode are indicated by the red, yellow and blue curves, shown in Fig. 6.25. It is obvious that under the proposed optimal modulation the BDC only operates with CPC modulation at the top end of the power range.

6.5 Evaluation of the Proposed Modulation

In order to evaluate the improvement achievable with the optimal modulation scheme in comparison with CPC modulation, the detailed bidirectional converter system has been simulated using the SLPS simulator. Here, the BDC circuit is simulated in PSpice (see Appendix K, Fig. K.1), while the controller algorithm (see Appendix M), the UC model (see Section 2.3.3), the PWM circuit (see Fig. 6.27), and the measurement circuits are modelled in Simulink, as shown in Fig. 6.26.

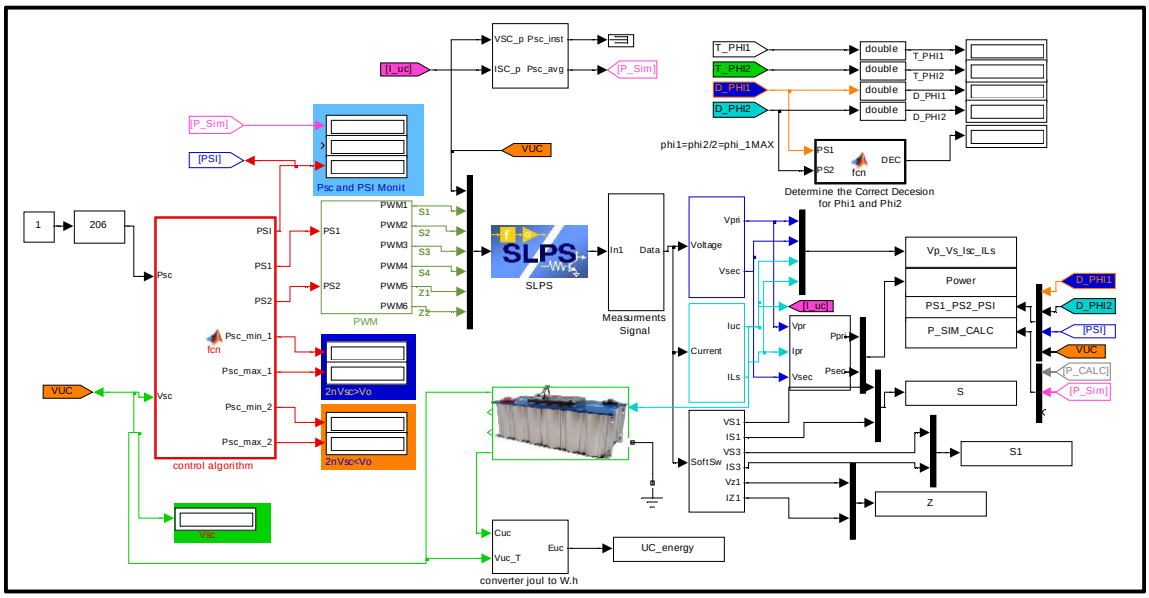


Fig. 6.26 PSpice/Matlab co-simulation for verifying the control algorithm of the proposed optimal modulation with the BDC

Fig. 6.26 shows that the control algorithm for optimal modulation scheme is built as an embedded function to generate the required phase-shift angles[15] (see Appendix M) for the PWM circuit depicted in Fig. 6.27.

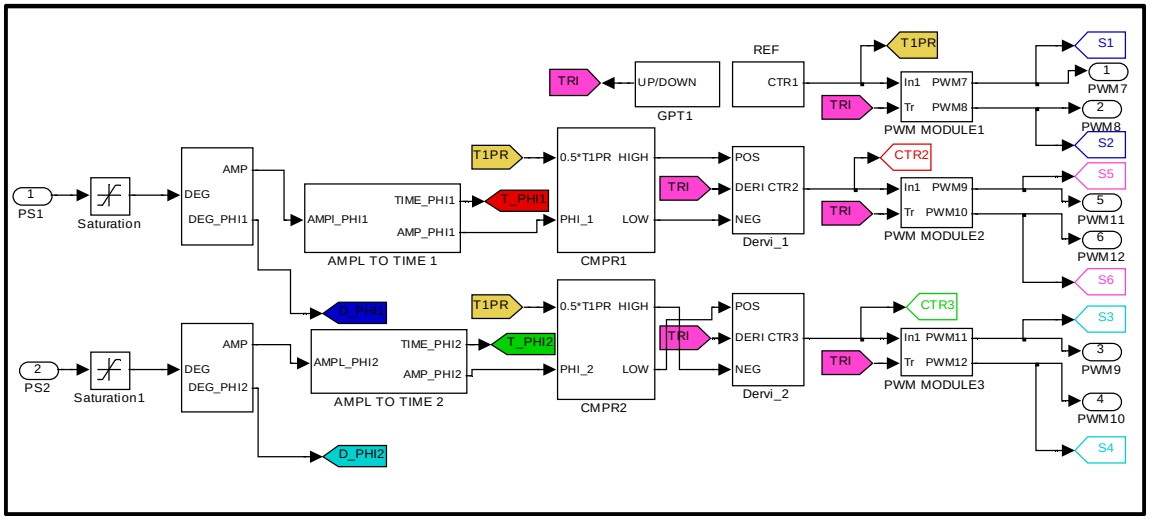


Fig. 6.27 Schematic block diagram of the PWM generation block in Fig. 6.26.

[15] Note that phase-shift angles φ_1 and φ_2 are denoted as PS1 and PS2 in the embedded function and PWM blocks while the CPF interval ψ is denoted as PSI.

The PWM generation block in Fig. 6.26 is shown in details in Fig. 6.27[16]. The implementation method to produce the required PWM signals for the BDC switches, the operation of the developed simulation model, and further details of the blocks in Fig. 6.26 and Fig. 6.27 can be found in Appendix K.

Based on the simulation prototype in Fig. 6.26 and Fig. 6.27 and their blocks details in Appendices K and J, a number of an accurate simulation results are obtained as described below.

To start the evaluation, Fig. 6.28, Fig. 6.29, and Fig. 6.30 show the operation of the BDC with three different operating Modes I, II, and III in respect to the phase-shift angles range described in Section 6.2.1.1.

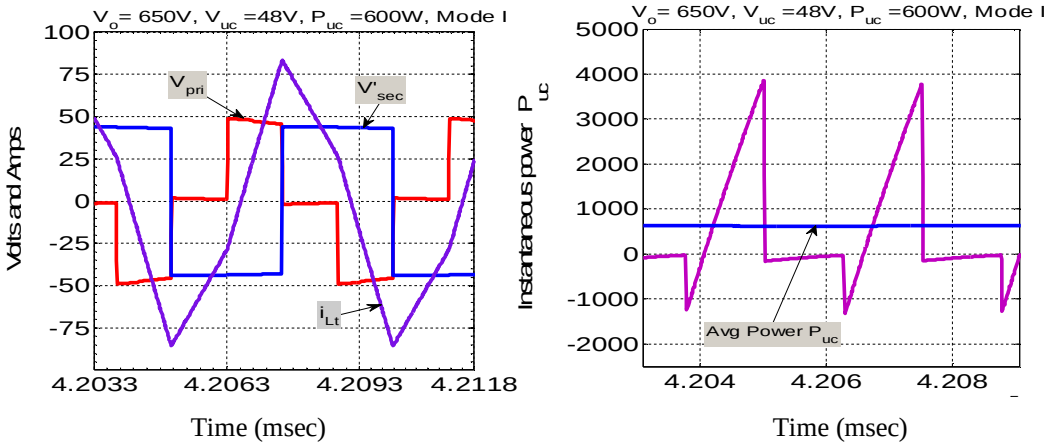


Fig. 6.28 Simulation waveforms for the BDC operation in Mode I (φ_1= 90^0 , φ_2=90^0) for $2nV_{uc} > V_o$ and UCDM: (a) voltage and current waveforms of the transformer (b) instantaneous and average power waveforms

[16] Because the control algorithm is to be implemented on the DSP, the generic names of the PWM module of the TMS320f2812 DSP are used in the simulation blocks diagram.

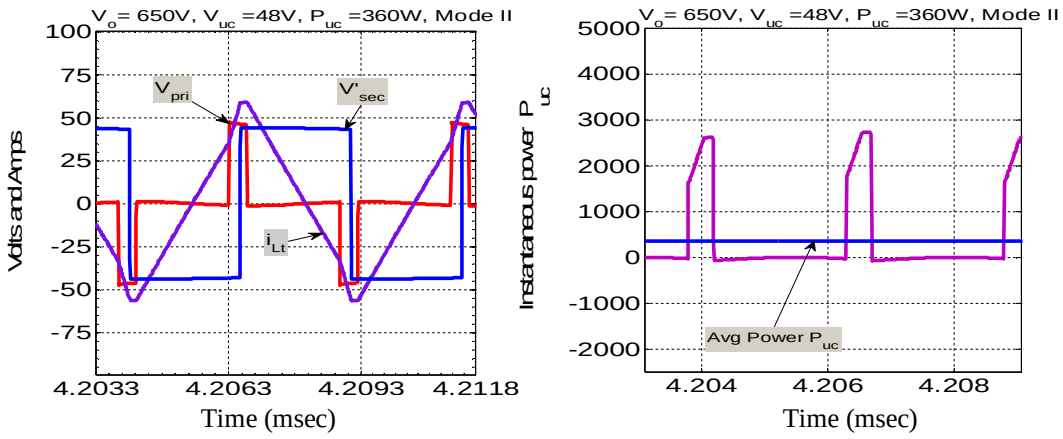


Fig. 6.29 Simulation waveforms for the BDC operation in Mode II (φ_1=20^0 ,φ_2=30^0, P_{uc}= 360W) for $2nV_{uc} > V_o$ and UCDM: (a) voltage and current waveforms of the transformer (b) instantaneous and average power waveforms

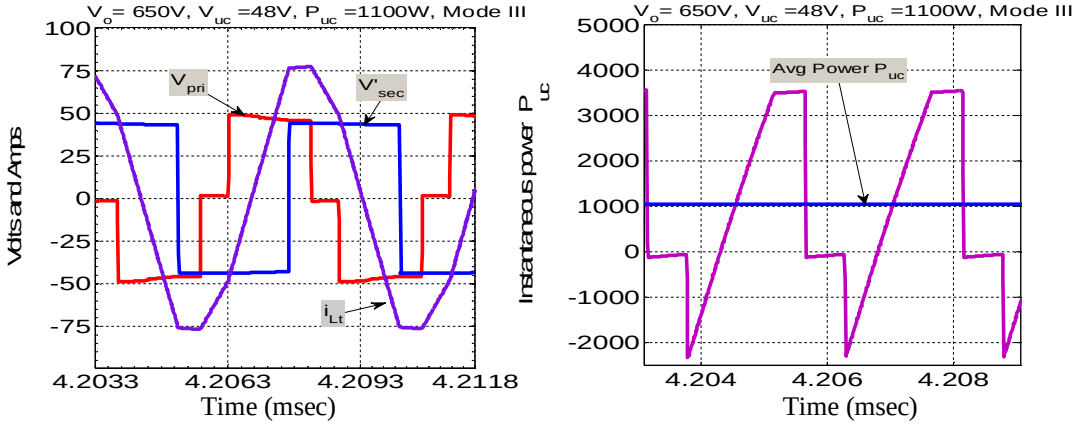


Fig. 6.30 Simulation waveforms for the BDC operation in Mode III (φ_1= 100 ,φ_2= 135, P_{uc}= 1100W) for $2nV_{uc} > V_o$ and UCDM: (a) voltage and current waveforms of the transformer (b) instantaneous and average power waveforms

The simulation results confirm the theoretical analysis that the operation of the BDC with the phase-shift angle range of these modes is not optimum due the high RMS and peak currents (see Fig. 6.28a, Fig. 6.29a, and Fig. 6.30a) and the HSW operation for the BDC switches.

In Fig. 6.31–Fig. 6.36 the simulation waveforms for BDC operation with the ZCPF modulation for different UC voltages and power levels and directions are depicted.

In addition to the voltages and currents in the primary and secondary windings (Fig. 6.31–Fig. 6.36a) the waveforms for the switching devices are also displayed (Fig.

6.31–Fig. 6.36 b, c, and d) to demonstrate the soft–switching operation of the BDC, while the waveforms of the instantaneous power (Fig. 6.31–Fig. 6.36e) show the absence of the circulating power flow.

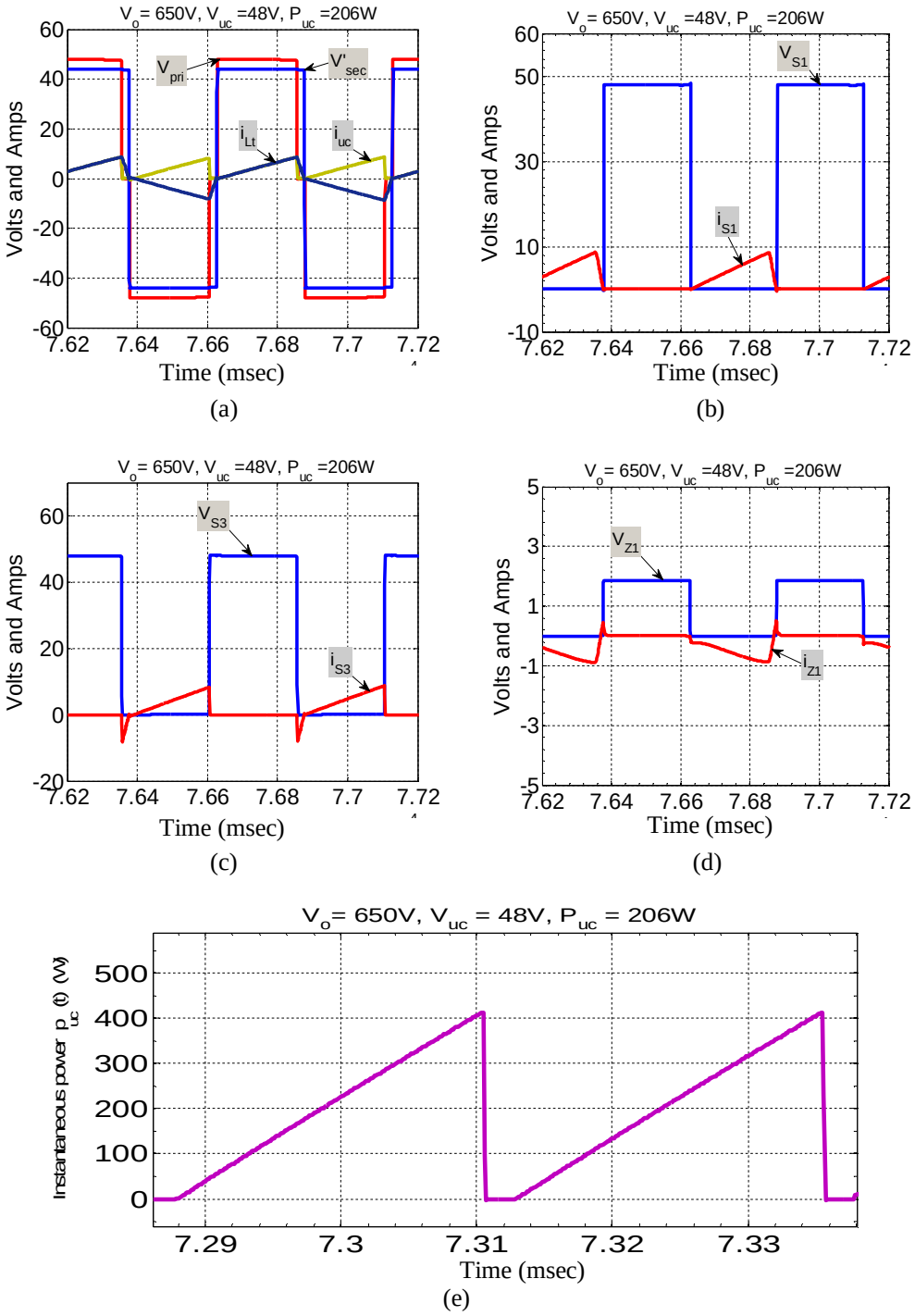


Fig. 6.31 Simulation waveforms for the BDC operation with the ZCPF mode for low power transfer ($\varphi_1 = 0^0$, $\varphi_2 = 164.7^0$): (a)-(d) voltage and current waveforms of the transformer and BDC switches, (e) instantaneous power waveform when the power transfers from the UC side to the DC-link side (n=7.4, L_t =10μH, f_s =20kHz, $2nV_{uc} > V_o$)

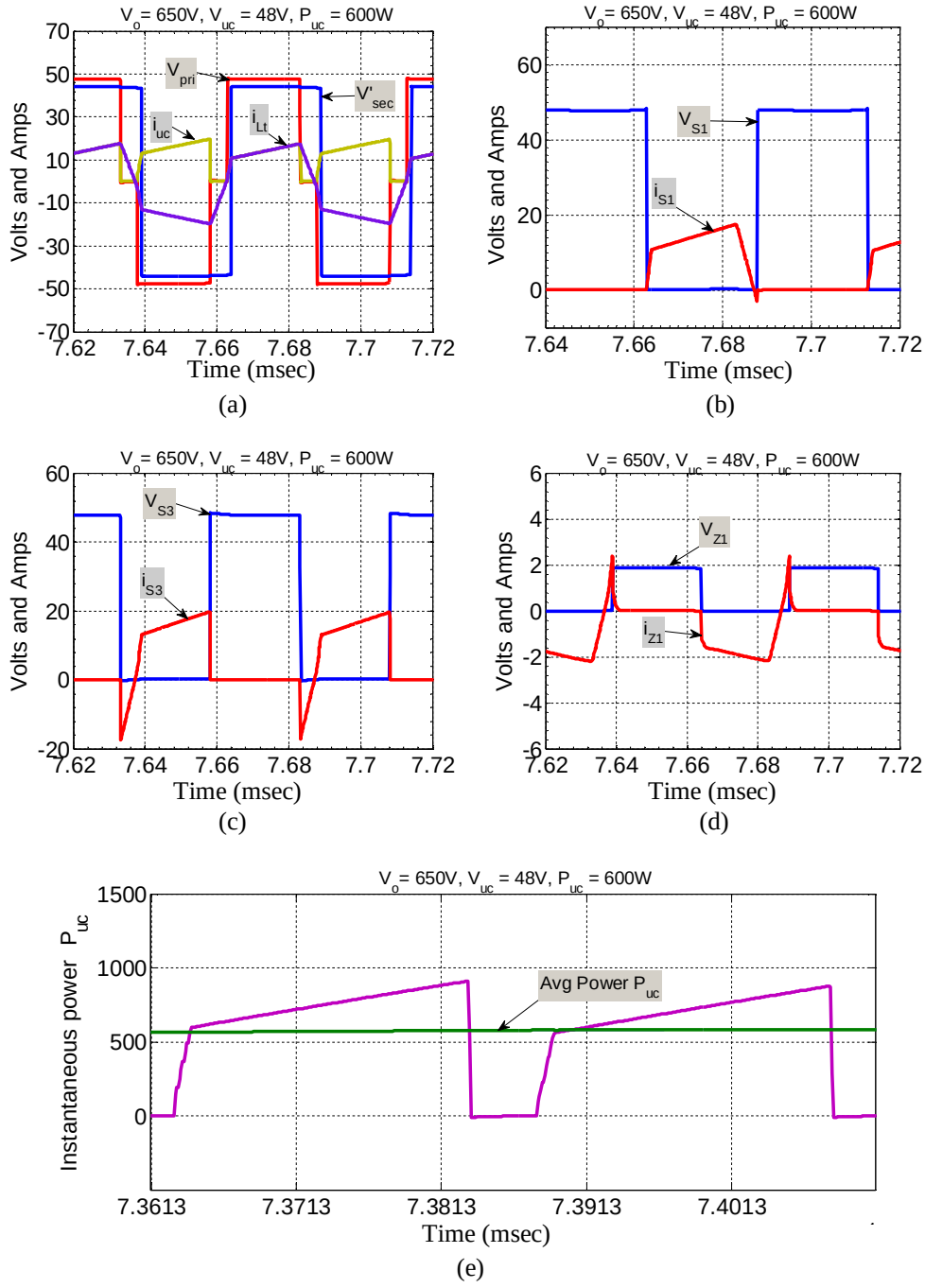


Fig. 6.32 Simulation waveforms for the BDC operation with the ZCPF mode for medium power transfer ($\varphi_1 = 9.4^0$, $\varphi_2 = 147.6^0$): (a)-(d) voltage and current waveforms of the transformer and BDC switches, (e) instantaneous power waveform when the power transfers from the UC side to the DC-link side (n=7.4, L_t =10μH, f_s =20kHz, $2nV_{uc} > V_o$)

Compared with the BDC operation in Mode I (Fig. 6.28a), a much less peak current through the converter can be observed in Fig. 6.32a. This confirms that the operation in Mode V can be considered as an optimum mode in respect of the lowest RMS and peak currents as expected in the theoretical analysis (see Section 6.2.1.1).

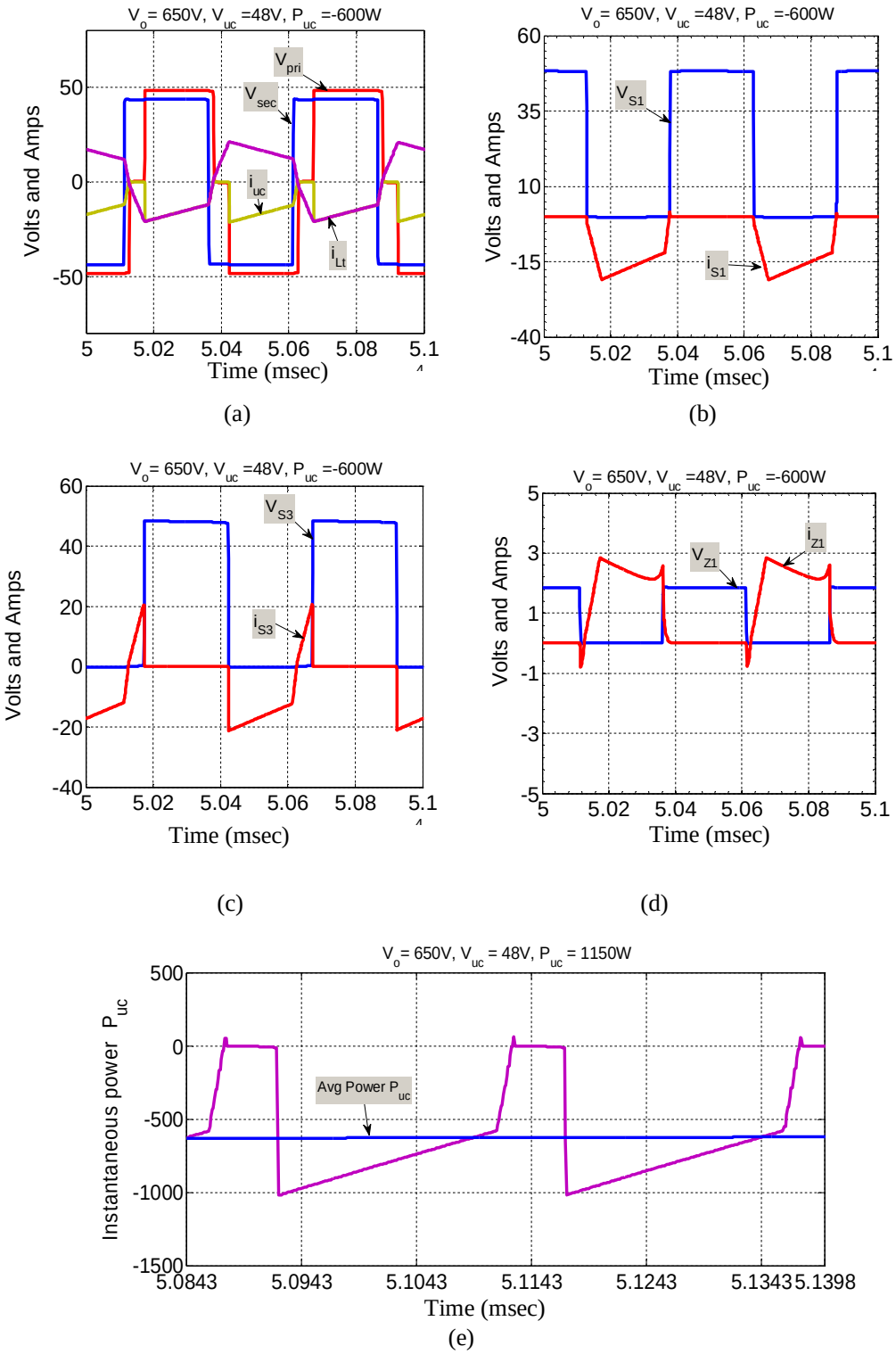


Fig. 6.33 Simulation waveforms for the BDC operation with the ZCPF mode (φ_1 =- 9.4^0, φ_2 = -147.6^0) when the power transfers from the DC-link side to the UC side (UCCM): (a)-(d) voltage and current waveforms of the transformer and BDC switches, (e) instantaneous power waveform (n=7.4, L_t =10μH, f_s =20kHz, $2nV_{uc} > V_o$)

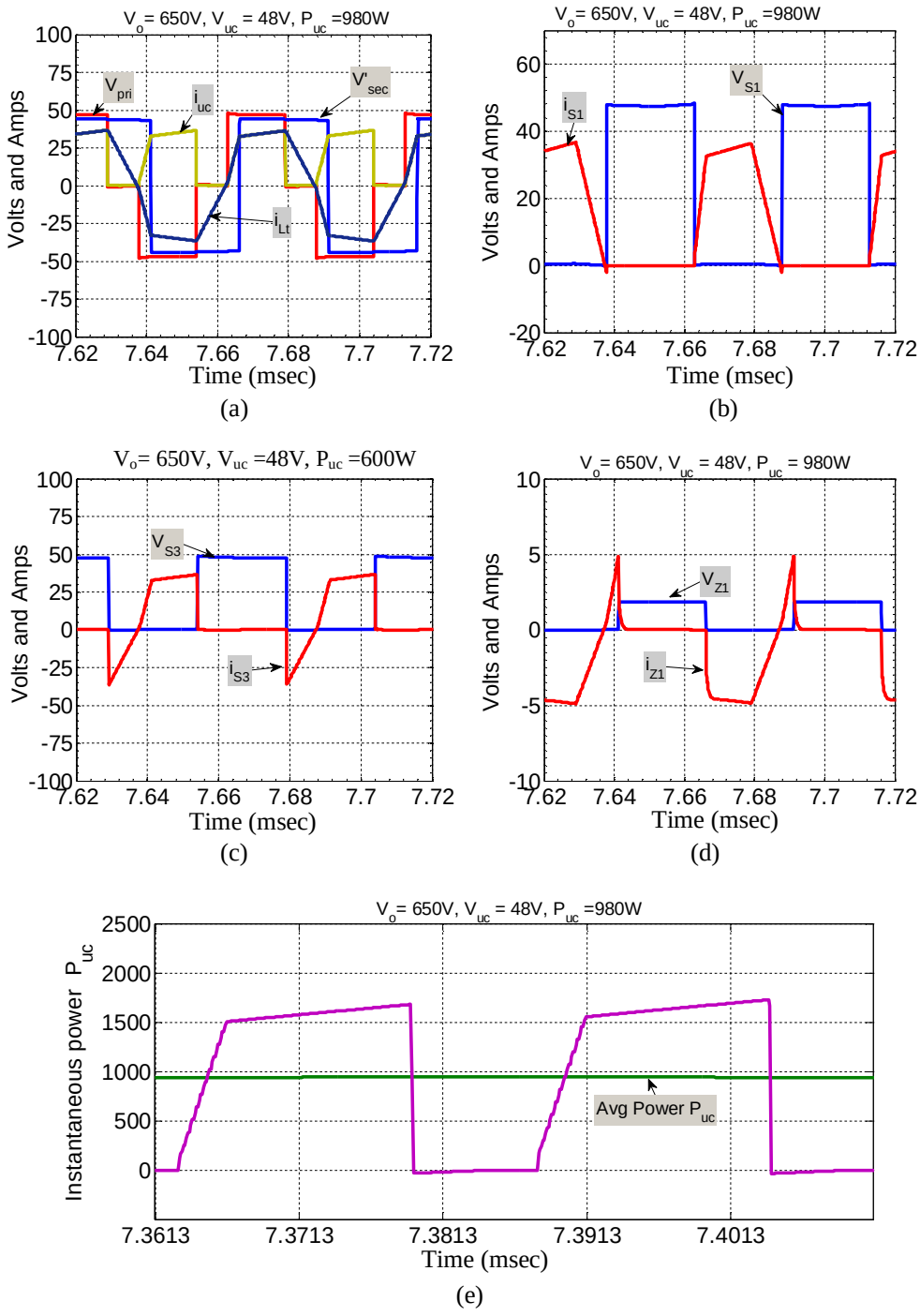


Fig. 6.34 Simulation waveforms for the BDC operation with the ZCPF mode for high power transfer ($\varphi_1 = 25.6^0$, $\varphi_2 = 117.8^0$): (a)-(d) voltage and current waveforms of the transformer and BDC switches, (e) instantaneous power waveform when the power transfers from the UC side to the DC-link side UCDM (n=7.4, L_t =10μH, f_s =20kHz, $2nV_{uc} > V_o$)

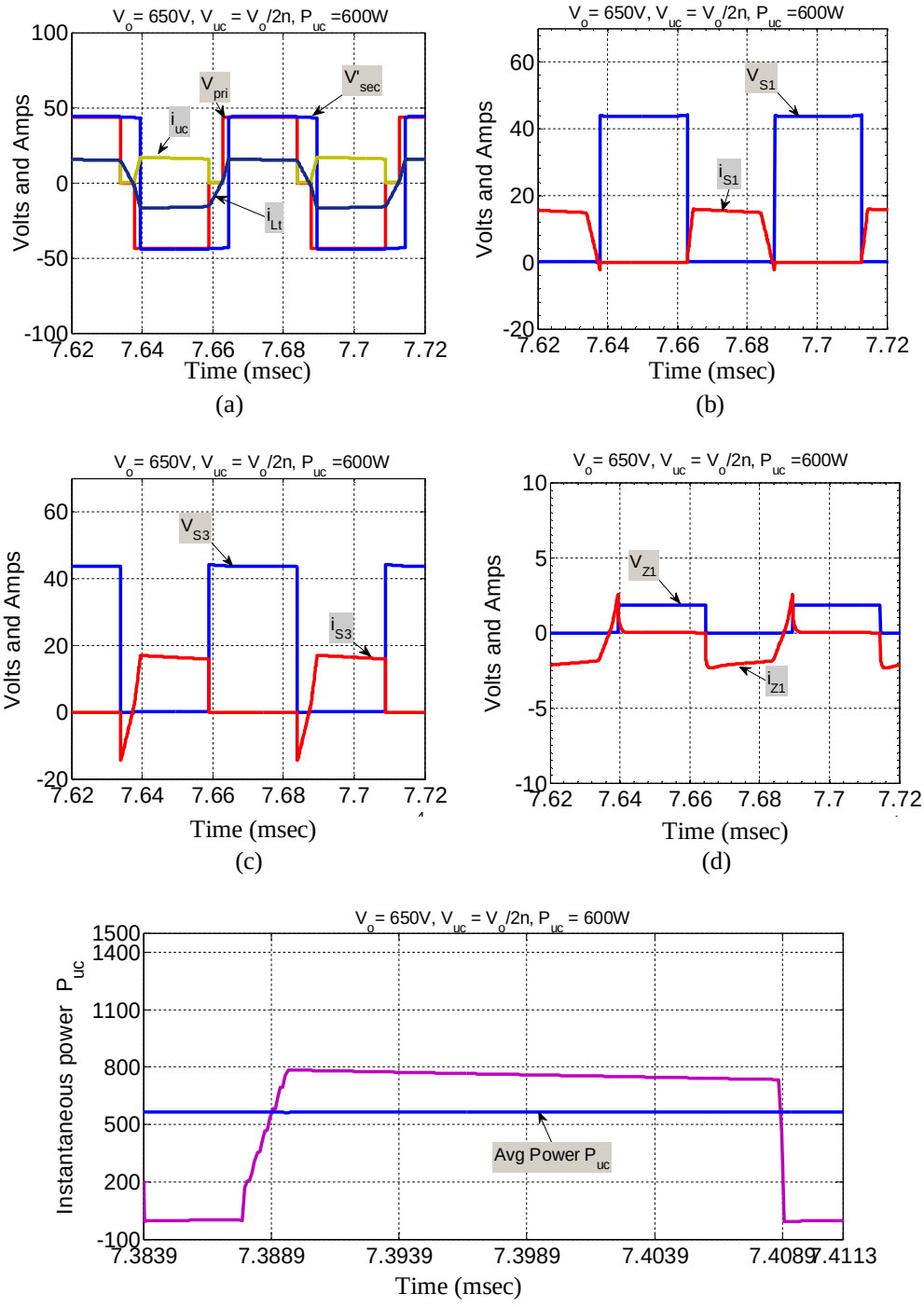


Fig. 6.35 Simulation waveforms for the BDC operation with the ZCPF mode when $2nV_{uc} = V_o$ (φ_1 = 13.87, $\varphi_2 = 152.3^0$): (a)-(d) voltage and current waveforms of the transformer and BDC switches, (e) instantaneous power waveform when the power transfers from the UC side to the DC-link side UCDM (n=7.4, L_t =10μH, f_s =20kHz, $2nV_{uc} = V_o$)

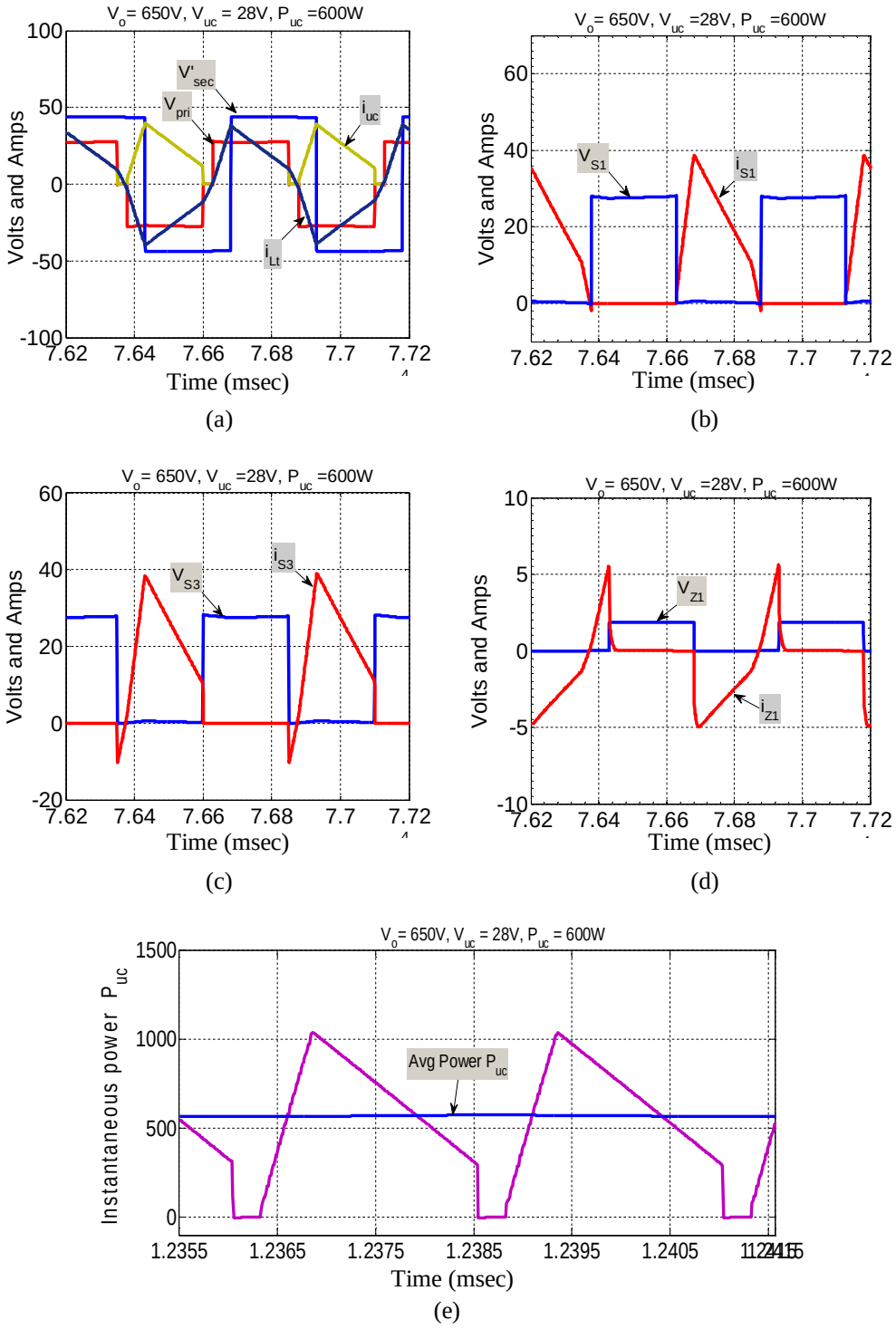


Fig. 6.36 Simulation waveforms for the BDC operation with the ZCPF mode when $2nV_{uc} < V_o$ ($\varphi_1 = 39$, $\varphi_2 = 159.9^0$): (a)-(d) voltage and current waveforms of the transformer and BDC switches, (e) instantaneous power waveform when the power transfers from the UC side to the DC-link side UCDM (n=7.4, L_t =10μH, f_s =20kHz, $2nV_{uc} < V_o$)

It can be noted in Fig. 6.31–Fig. 6.36b that the switch S_1/S_2 turned on and turned off with ZCS for any UC voltage (see Fig. 6.32b, Fig. 6.35b, and Fig. 6.36b) and for both power flow directions (see Fig. 6.33b). The same for the switches S_3/S_4 and Z_1/Z_2 are turned on with ZVS for wide UC voltage variation and for both UCDM and UCCM operation (see Fig. 6.32c-d, Fig. 6.35c-d, Fig. 6.36c-d, and Fig. 6.33c-d).

The instantaneous power waveforms in Fig. 6.31–Fig. 6.36e depict that the BDC can be operated with zero CPF interval during the ZCPF mode for both power transfer directions (Fig. 6.33e) and when $2nV_{uc} > V_o$ (Fig. 6.32e), $2nV_{uc} = V_o$ (Fig. 6.35e), and $2nV_{uc} < V_o$ (Fig. 6.36e) over a wide power range (see Fig. 6.31e and Fig. 6.34e).

Simulation of the BDC operation with the ISP and MCPF modes is shown in Fig. 6.37 and Fig. 6.38. Compared with CPC modulation, the CPF interval is reduced (see Fig. 6.37e and Fig. 6.38e). This has impact of reducing the RMS and peak currents as indicated in Fig. 6.23.

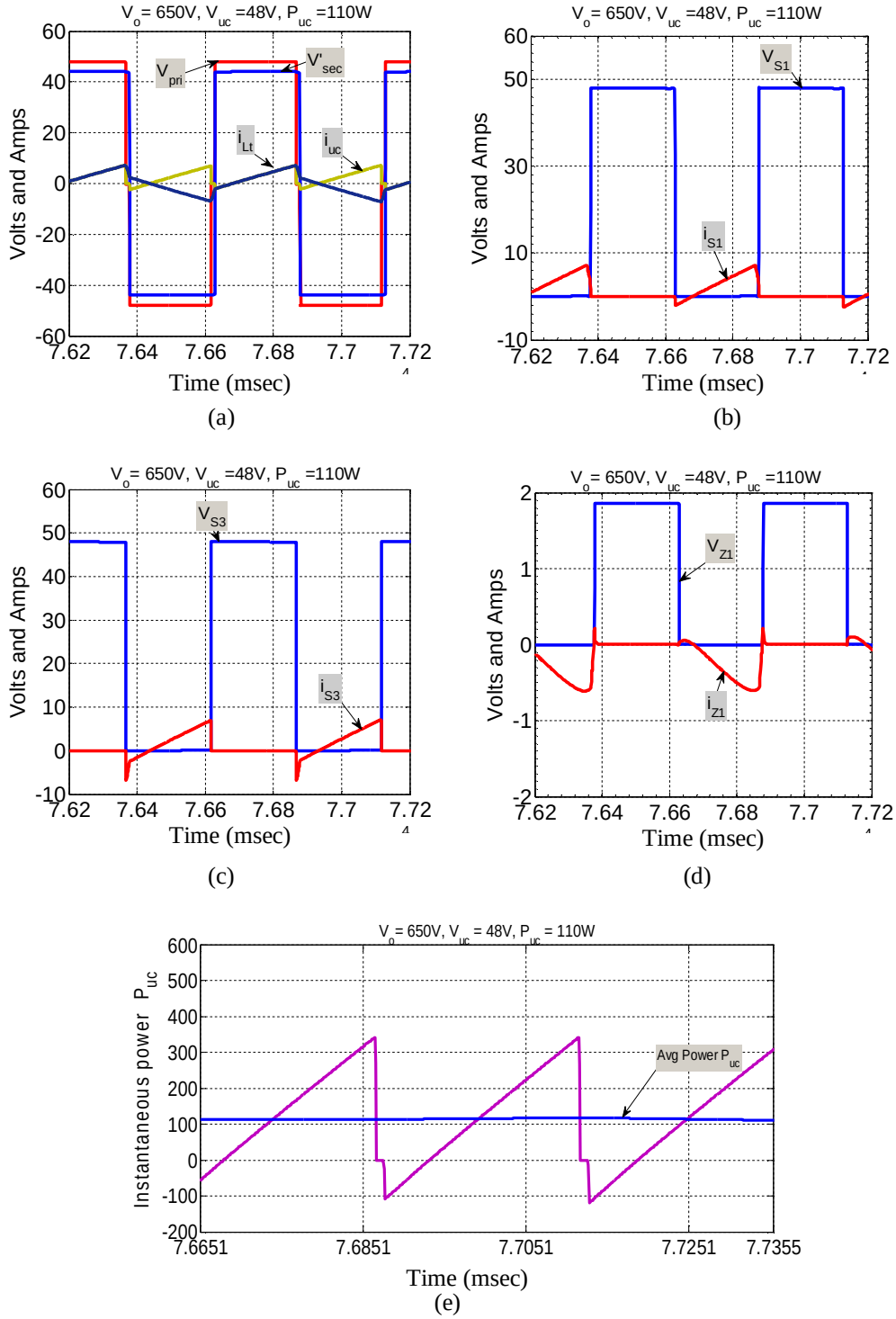


Fig. 6.37 Simulation waveforms for the BDC operation with the ISP mode when $2nV_{uc} > V_o$ ($\varphi_1 = 0$, $\varphi_2 = 172.1^0$ $\psi = 1.9^0$): (a)-(d) voltage and current waveforms of the transformer and BDC switches, (e) instantaneous power waveform when the power transfers from the UC side to the DC-link side UCDM (n=7.4, L_t =10μH, f_s =20kHz)

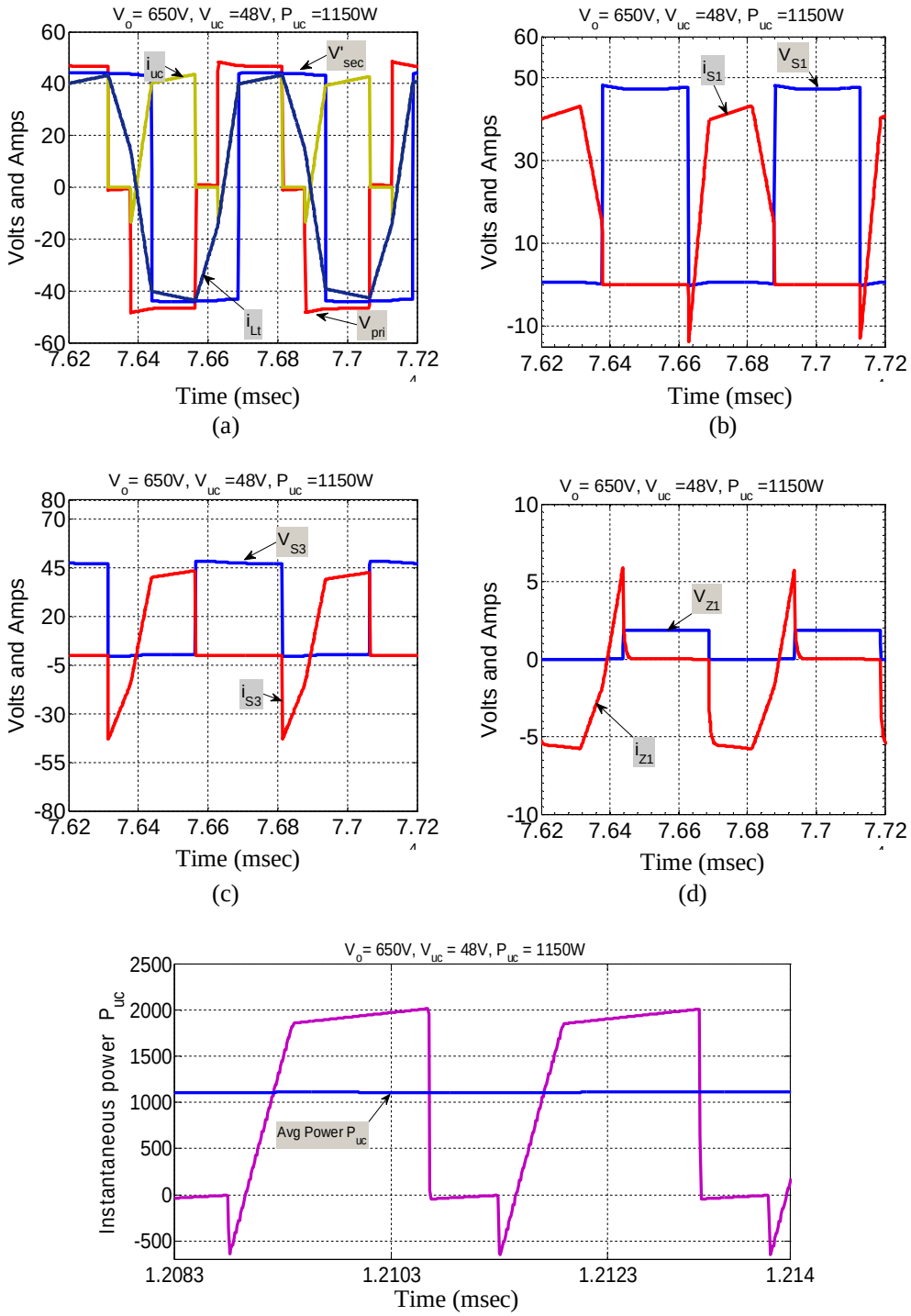


Fig. 6.38 Simulation waveforms for the BDC operation with the MCPF mode when $2nV_{uc} > V_o$ ($\varphi_1 = 44.61^0$, $\varphi_2 = 134.6^0$ $\psi = 13.46^0$): (a)-(d) voltage and current waveforms of the transformer and BDC switches, (e) instantaneous power waveform when the power transfers from the UC side to the DC-link side UCDM (n=7.4, L_t =10μH, f_s =20kHz)

Similar to ZCPFM, both ISPM and MCPFM are exhibiting a SSW operation over a wide UC voltage variation as demonstrated in Fig. 6.37b-d and Fig. 6.38b-d. Thus, the SSW operation of the BDC with the proposed optimal modulation scheme is not restricted by the UC voltage changes unlike that shown with the CPC modulation (see Section 5.2). Table 6.5 summarises the SSW operation of the BDC under the optimal modulation scheme for UCDM operation.

TABLE 6.5
SOFT-SWITCHING STATUS FOR THE PROPOSED MODULATION SCHEME

		$P_{uc} > 0$ and $2nV_{uc} > V_o$		$P_{uc} > 0$ and $2nV_{uc} < V_o$	
Schemes	States	ZVS	ZCS	ZVS	ZCS
ISPM	0	S_1 on	Z_1on	S_1 on	Z_1on
	φ_1				
	φ_2	S_3on		S_3on	
	π	S_2 on,	Z_2on	S_2 on,	Z_2on
ZCPFM	0		S_1 on S_2off		S_1 on S_2off
	φ_1	Z_1 on		Z_1 on	
	φ_2	S_3on		S_3on	
	π		S_1 off S_2 on		S_1 off S_2 on
	$\pi+\varphi_1$	Z_2 on		Z_2 on	
	$\pi+\varphi_2$	S_4on		S_4on	
MCPFM	0	S_1 on		S_1 on	
	φ_1	Z_1 on		Z_1 on	
	φ_2	S_3on		S_3on	
	π	S_2on		S_2on	

As demonstrated in Fig. 6.39, a significant improvement in the efficiency is achieved with the ISPM and ZCPFM. The reason for this is the reduction of the peak and RMS currents through the switching devices and the transformer as well as the soft-switching operation. Unlike with the TRM, PTRM, TZM, and MTRM methods it can be seen from the presented waveforms that with the proposed method the primary current is continuous over the entire power range, which results in lower peak currents.

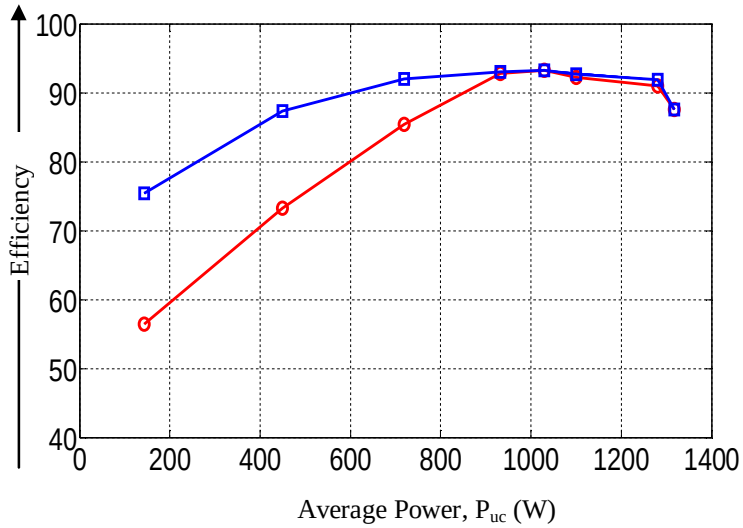


Fig. 6.39 Simulated efficiency of the BDC with the proposed modulation (blue) compared to the CPC modulation (red) for $2nV_{uc} > V_o$ and $P_{uc} > 0$ (UCDM)

In addition, the simulation results in Fig. 6.40 confirm the theoretical analysis in Section 6.4.4 that the proposed modulation scheme shows a seamless transition between the operating modes, where the power changes without chattering. Implementation of the controller is also simplified because no hysteresis block is required to select the appropriate mode.

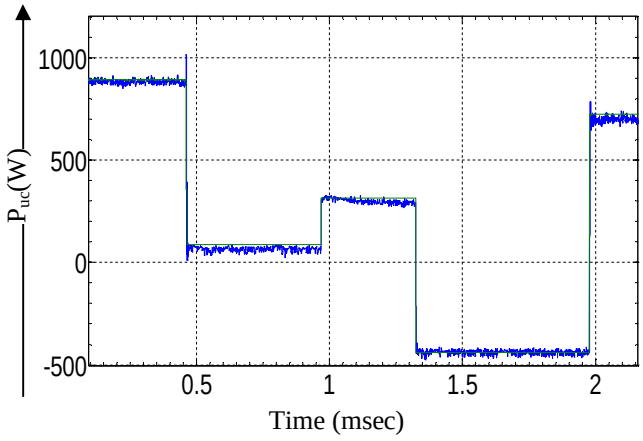


Fig. 6.40 BDC power changes (green: calculated; blue: simulated)

Similar to the verification methods used in Chapter 4, the fidelity of the BDC with the controller algorithm has been verified using the PCM approach and the new SLPS-PIL

dual co-simulation[17] (see Section 4.6.3.1 for more details). Fig. 6.41 shows the average power of the BDC obtained by two simulation approaches. As can be seen a good matching between the simulation results is achieved which confirms the validity of the controller algorithm of the proposed optimal modulation scheme.

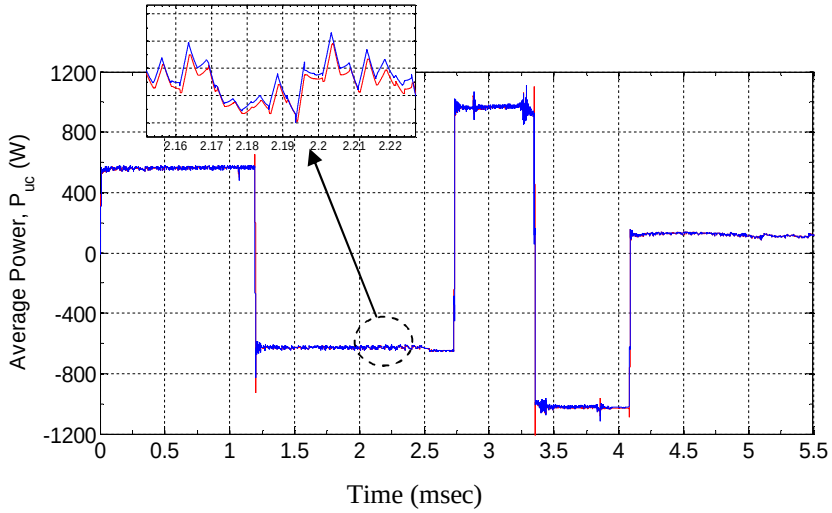


Fig. 6.41 PCM approach results (blue) against SLPS-PIL dual co-simulation results (red)

Simulation of the whole UC–BDC system for different output power levels and for fully charging and discharging the UC is shown in Fig. 6.42. It can be seen that the proposed optimal modulation scheme keeps the CPF interval ψ as low as possible without any discontinuities in the phase-shifts φ_1 and φ_2 for different UC voltages and power levels. These results confirm the mathematical analysis shown in Fig. 6.22.

[17] In order to verify the control algorithm of the optimal modulation method on the DSP using the PIL simulation, all the blocks of Fig. 6.27 are implemented as a fixed-point data type using IQ math and DMC libraries as shown in Appendix K, Fig. K.9.

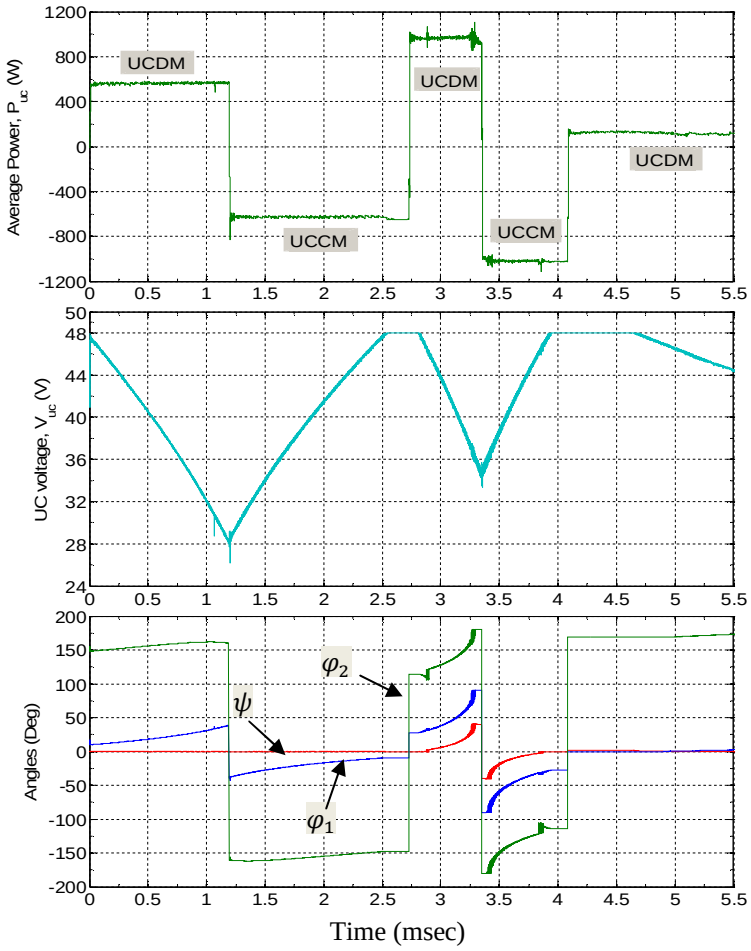


Fig. 6.42 Simulation results of the whole UC–BDC system with different power levels

The BDC shown in Fig. 5.1 was built in the laboratory using a layout and switching devices take in the account all the problems associated with the FC converter in Chapter 3. Fig. 6.43 shows a photograph of the prototype converter, while the schematic circuit diagrams of the converter, MOSFETs and IGBTs driver circuits, and DSP–PWM interfacing circuit are shown in Appendix L. Unfortunately, due to time restrictions no practical results were available at the time of writing this thesis.

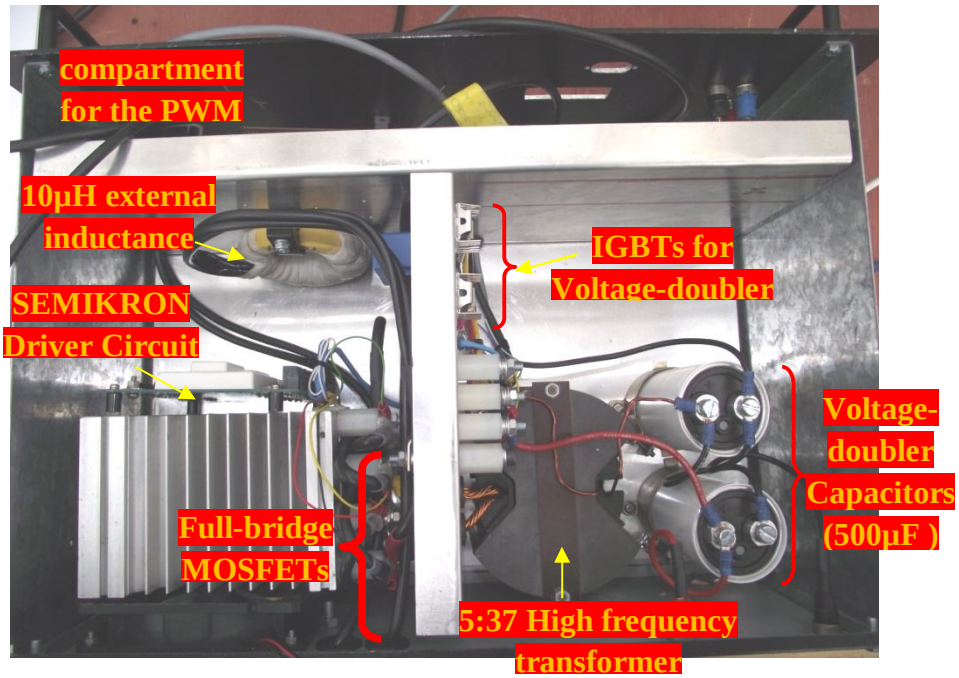


Fig. 6.43 The prototype of the BDC

6.6 Conclusions

It has been demonstrated that a circulating power flow is the main source of high RMS currents, conduction losses and current ripple in the phase-shifted bidirectional DC-DC converter. The circulating power flow interval is related to the power required by the load and the input voltage and is an intrinsic property if the CPC modulation is employed. This chapter has presented a new modulation scheme to minimise the circulating power flow interval in the bidirectional DC-DC converter for an ultracapacitor energy buffer. The proposed scheme decreases the circulating power flow to zero over most of the power range and minimises it over the remainder of the range for a wide variation of the ultracapacitor voltage. In addition, the proposed modulation shows an increase in the soft-switching range and achieves a seamless transition between the proposed modes as the power required is increased. Compared to the TRM, PTRM, MTRM, and TZM methods described in [19, 122, 127, 137, 142, 144, 148], the proposed modulation keeps the primary current continuous for the entire output power

range, resulting in lower RMS current and conduction losses. In comparison with CPC modulation the proposed modulation scheme results in higher converter efficiency. Furthermore, the new optimal modulation has been implemented with a switching control strategy, using a fixed 50% duty cycle for the switches on both sides of the converter. Thus, this method simplifies implementation of the control algorithm since no duty cycle variation is needed.

Chapter Seven

Conclusions, Original Contributions and Suggestions for Future Work

This Chapter summarises the conclusions that are drawn from this research work and describes the main contributions of this study along with suggestions for future work.

7.1 General Conclusions

The main features of the power electronic converters in the DC microgrid are to facilitate the integration of different renewable energy resources to the DC bus-bar of a DC microgrid, optimise the management of the power flow between the generators, the loads and the utility grid, effectively utilise the supplied power from the renewable energy resources, and provide a reasonable power quality to the loads, even with high penetrations of renewable energy. However, more converters may lead to degradation in the microgrid efficiency. Thus, to further improve the DC microgrid performance and efficiency, the aim of this research was to develop and implement high efficiency DC–DC converter topologies for a FC–UC DC microgrid that take into account the output characteristics and the dynamic response of the resources in the design stage. To this aim the detailed dynamic performance of these resources has been examined first after which suitable converters are proposed and selected. A number of optimisation steps were taken to further improve the performance of the proposed FC converter; while a novel modulation scheme has been presented to control the power flow of the UC converter with minimum losses over the entire range of load and UC voltage variations.

To evaluate the proposed improvements which can be achieved on the DC microgrid, the presented FC converter system was tested in the laboratory, while the UC converter was validated using the detailed mathematical analysis and simulation results.

7.2 Original Contributions

The new contributions of this work can be found in the following aspects:

- An appropriate selection of power conditioning unit required for interfacing of FC and UC onto the DC bus-bar of a DC microgrid in respect to the dynamic response of these resources is a significant technical challenge. However, the research presented here has shown that, with a comprehensive overview on different topologies, unidirectional current–fed converter provides the best solution to achieve most of the properties required for the FC, whilst bidirectional voltage–fed converter is better suited for dealing with the fast dynamic response of the UC. In that context, selection of suitable converter topology was achieved.

- The MOSFET conduction losses are the dominant factor in the converter efficiency. The On-resistance of a MOSFET, which determines the conduction losses of the MOSFET, increases proportionally with the voltage rating. Unfortunately, a high voltage stress across the switches is the main drawback of the current–fed topologies. Therefore, an active clamp circuit is often implemented to suppress any voltage overshoot across the switches. But, an active clamp circuit can lead to high circulating energy that adds to the conduction losses of the converter. In addition, the resonant between the clamp capacitance and the transformer leakage inductance can result in an increase in

the clamped voltage level across the primary winding and the switching devices which has a negative impact on the converter efficiency. In this work, a new current–fed converter design with a low voltage rating of the switches and high voltage conversion ratio is proposed. By combining the active clamp circuit with the voltage-doubler technology a reduction has been achieved in the voltage rating of the switches and the energy circulation through the converter reaches up to 50% less than other competing current–fed topologies. The converter achieves soft-switching, low input current ripple and a high efficiency over the whole load range, which is very attractive for the FC. An innovative optimisation approach for the design of the active clamp circuit has been proposed to further improve the converter performance and efficiency. The steady–steady and dynamic performance of a novel topology has been verified by the detailed simulation and experiment in comparison to other competing configurations.

- The current-fed converter with active clamp circuit has promising features for reducing the voltage stress across the converter switches and achieving ZVS. It was found that parasitic elements of the converter can have a large impact on the efficiency of current-fed converters with an active clamp. This has not been reported in the literature. In this work it has been shown that particularly during the switch overlap period the parasitic elements create undesirable oscillations leading to additional circulating energy which adds to the conduction losses of the converter. It also results in voltage ringing across the clamp switch, oscillations in the current through the clamp circuit and high voltages across the bridge switches, even when the switches are conducting. Based on this finding a

number of modifications have been proposed and these have been verified by experiment.

- For the study of the dynamic behaviour of the proposed converter and the design the required controller, a dynamic model for the converter is necessary. A detailed small-signal control-oriented model of the converter has been developed, which includes the active-clamp circuit, the FC power source, and the dynamic impact of the parasitic elements. The dynamic model presented in this work has been utilised to systematically design a digital average current-mode controller for the FC power converter system. The functionality of the controller system executed on the real processor hardware and the performance of the FC converter has been validated using the model-based design approach.

- Computer models that accurately simulate the behaviour of a power electronic converter in conjunction with the dynamics of its input source and feedback controller would be of high value. However, most of today's models cannot capture accurately the dynamic performance of power electronic circuits. To address this, a new approach has been developed in this work based on the integration of three simulator packages via two interfacing software programs; two of these simulators (PSpice and Simulink) are used to execute the model of the physical components of the converter, and its input source on the PC host, while the third simulator executes the digital controller algorithm on the actual processor hardware. This novel approach provides a unique test method to validate the code of the controller algorithm on the real processor which controls a virtual prototype of a converter system. The results using this approach have been validated with experimental results.

- A number of modulation schemes have been presented in the literature to improve the efficiency, reduce the switching and conduction losses and control the power flow in a bidirectional converter. A comparative study to classify the advantages, disadvantages, features, and the applicability of these methods for the UC applications are presented in this work.

- The dominant losses that have a major impact on the converter efficiency for the low-voltage high-current applications are the conduction losses. The circulating power flow in the bidirectional converter is shown to have a major effect on increasing the conduction losses. However, analytical work to define and understand the impact of circulating power flow on the steady-state operation of the bidirectional converter has only been reported using a fundamental component approximation. In this work, it has been shown that circulating power occurs during certain intervals in the cycle depending on the power demand and the UC voltage. Therefore, a detailed analysis of the bidirectional converter exploring the impact of the circulating power flow interval is developed in this research. Based on the definition of circulating power flow, the equations that determine the duration of circulating power flow interval have been derived. The in-depth analysis on the bidirectional converter has led to new analytical expressions for the RMS current and power flow transfer. A novel optimal modulation scheme, based on finding the minimum duration of this interval, has been proposed and verified by a comprehensive mathematical analysis and detailed simulation. Furthermore, the proposed method has been implemented with a switching control strategy, using a fixed duty cycle for the switches on both sides of the converter.

7.3 Suggestions for Future Work

This thesis contributes to improve the performance of the power electronic converters for a DC microgrid particularly for the FC and UC sources. Based on the results of this work the following recommendations for further research are suggested:

- The proposed FC current–fed converter is operating with a wide soft-switching range for both converter sides but its full bridge switches still suffer from hard switching operation at turn-off. Further investigation and study need to be carried out on the converter to turn off the switches with either ZVS or ZCS. However, this should be achieved without increasing the converter component count.

- The optimal modulation schemes presented in Chapter 6 for the UC bidirectional converter should be tested experimentally to verify the practical efficiency improvement that have been achieved using this modulation method.

- The modulation schemes presented in Chapter 6 have assumed that the DC link voltage is a constant. In a future step, the discussed method needs to be extended to take into account the effect of the DC link voltage variation on the calculated phase–shift angles. In addition the effect of the dead time between the bridge switches in the same leg and the rise and fall times of the gate signals can be included in the detailed mathematical analysis that was applied to find the optimum phase–shift angles. This allows to cover all factors that influence the correct phase–shift angles for obtaining zero or minimum circulating power flow.

- Further research in the modelling and control of the power management for the FC–UC DC microgrid is needed. The developed control strategy described in Section 2.4.2 need to be adapted to include the controller algorithm that was proposed to optimise the BDC operation. In addition, the two phase–shifts should be considered separately when designing the control strategy.

Appendix A

FC Source Model Using Parameters Extracted from Measurements

A number of steady-state and dynamic models of the PEMFC have been reported in [151-153]. Some of the steady-state models use empirical equations and electrochemical reactions inside the FC to obtain the FC characteristics [154], while other models are based on the dynamics of the FC that affect the terminal characteristics of the PEMFC using an equivalent electrical circuit such as in [155]. Most studies do not consider the full modelling of all parameters of a particular FC stack. In Matlab/Simulink a generic model is available that represents most popular types of FC stack taking into account a number of FC parameters such as fuel and air pressures, temperatures, composition, flow rates of H_2 and air variations. The user can select between two versions of the stack model: a simplified model and a detailed model [156]. In this appendix the existing dynamic model of PEMFC, available in Matlab/Simulink, has been further developed and then validated with an experimental data shown in Section 2.2.4.2 by extracting some of the FC parameters from experiments results (see Table A.1).

TABLE A.1
EXTRACTED PARAMETERS FROM MEASURES RESULTS

FC Parameters	Value
Open circuit voltage	43V
Nominal operating voltage and current	26V, 46A
Maximum operating point	60A, 23V
Number of cells in stack	43
Nominal stack efficiency	40%
Operating temperature	30^0C
Nominal air flow rate	69 l/min

To obtain a dynamic response of the Simulink FC model that is as close as possible to that of the real FC stack, flow rate regulators to control the fuel and air utilization

shown in Fig. A.1 have been added to the model.

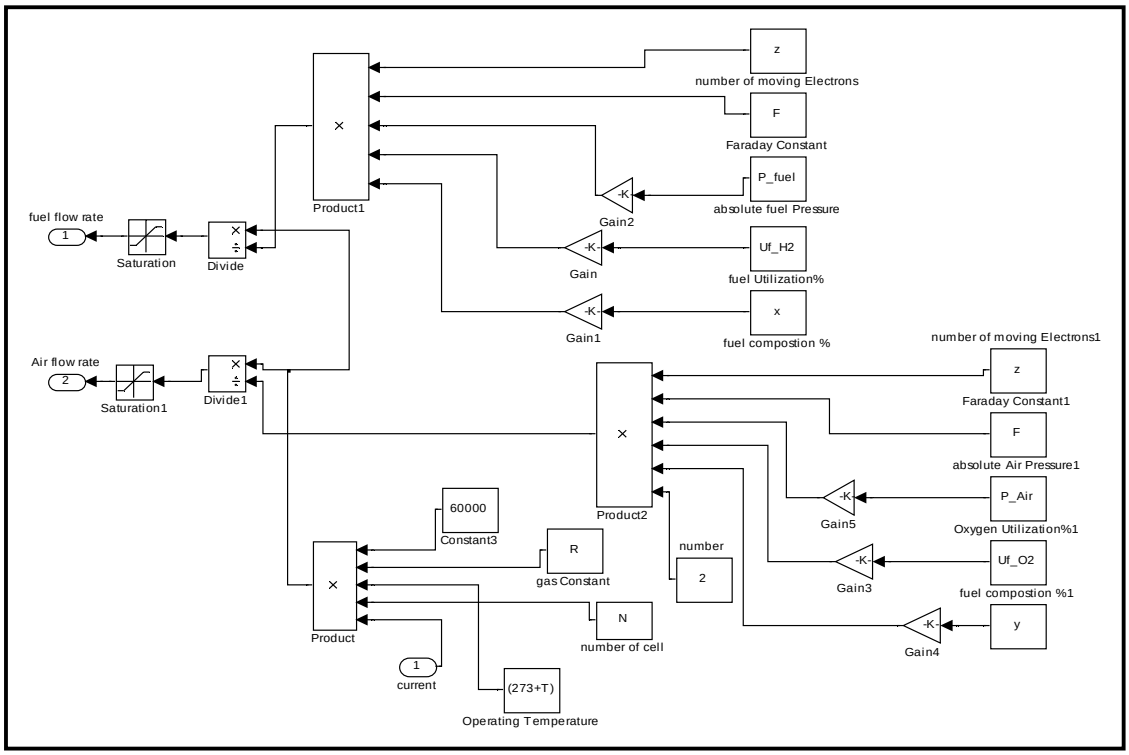


Fig. A.1 Fuel and air flow rates regulators

Using a resistance equal to 0.65Ω as a load with switches controlled by a timer at the same rate as in the experiment, the load demand can be changed as shown in Fig. A.2. An additional resistor R_p is connected across the FC terminals to represent the ancillary loads.

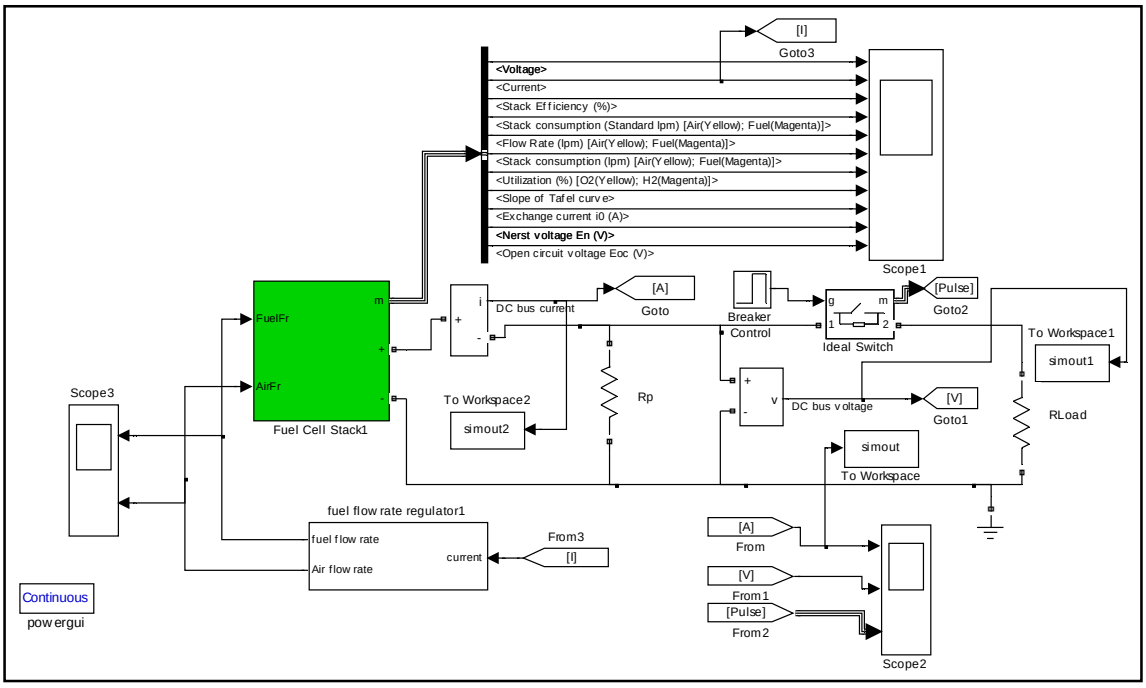
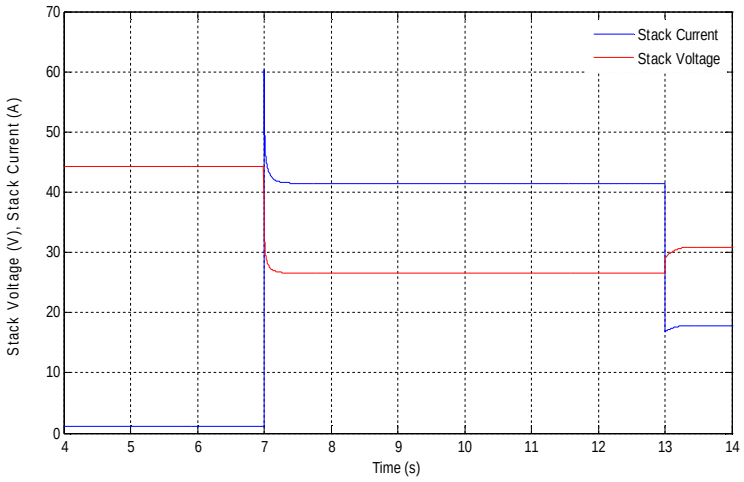
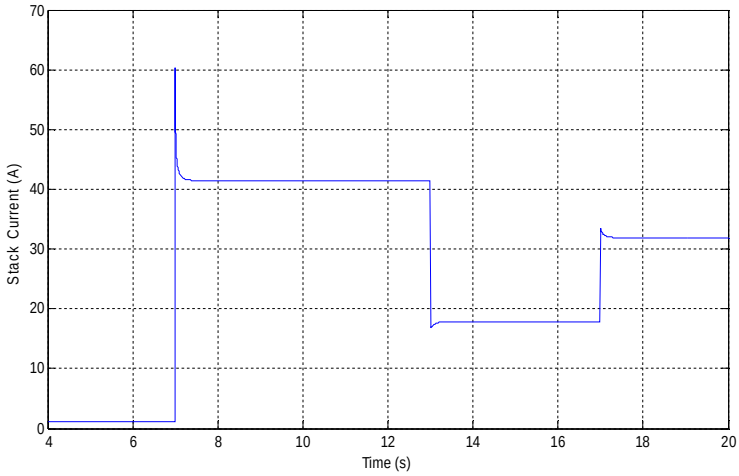


Fig. A.2 FC model test under resistive load

The transient response of the FC stack is shown in Fig. A.3(a). As can be seen from this figure, the current spike goes up to 60A when the load changes suddenly from no-load and the voltage drops to approx 26V just as in the measurements. Fig. A.3(b) demonstrates how the activation voltage drop changes when the load is changing more slowly. Fig. A.4 shows that the fuel and air flow regulators matches well with the real FC system results. In general, the Simulink results show that the modelling matches well with the experimentations set-up shown in Section 2.2.4.2.



(a)



(b)

Fig. A.3 Simulation results of the FC current and voltage (a) from no-load to full load (b) Simulation results of the FC current at different load-demands

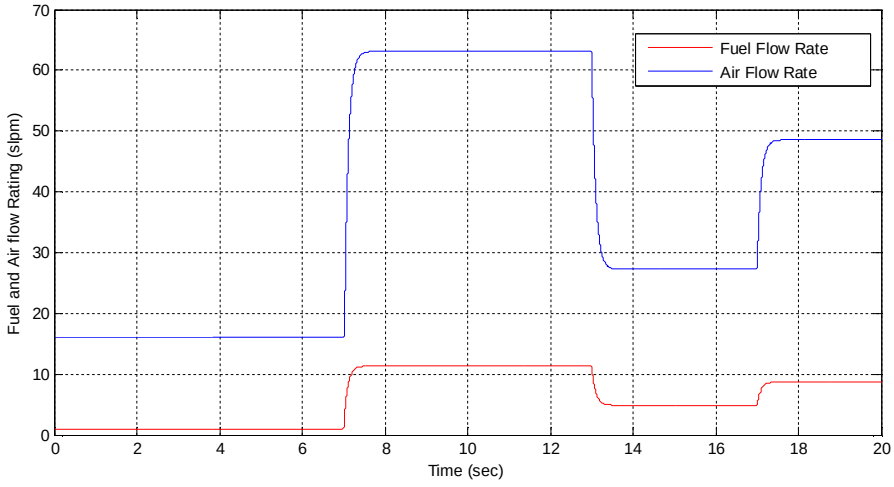


Fig. A.4 The simulation results of fuel and air flow rating with load changes

Appendix B

DSP–PWM Interface Circuit

As indicated in Appendix H, all the gate signals are generated in a DSP using one GP timer (see Fig. H.1). SKHI 22 B(s) drive circuits are used for the main and clamp MOSFETs. To get the required 40 kHz gate signal for the clamp switch S_c, PWM1 and PWM4 in the Compare Unit are used and then the two signals are combined using an 74HCHCT32 OR gate, as shown in Fig. B.1. To raise the 3.3V output voltage of the on-chip PWM of the DSP to the required 5V input signal voltage for the MOSFET gate driver, an MC74HC04ADR2(s) hex-inverter is used which acts simultaneously as a level shifter and as a buffer, as indicated in Fig. B.1.

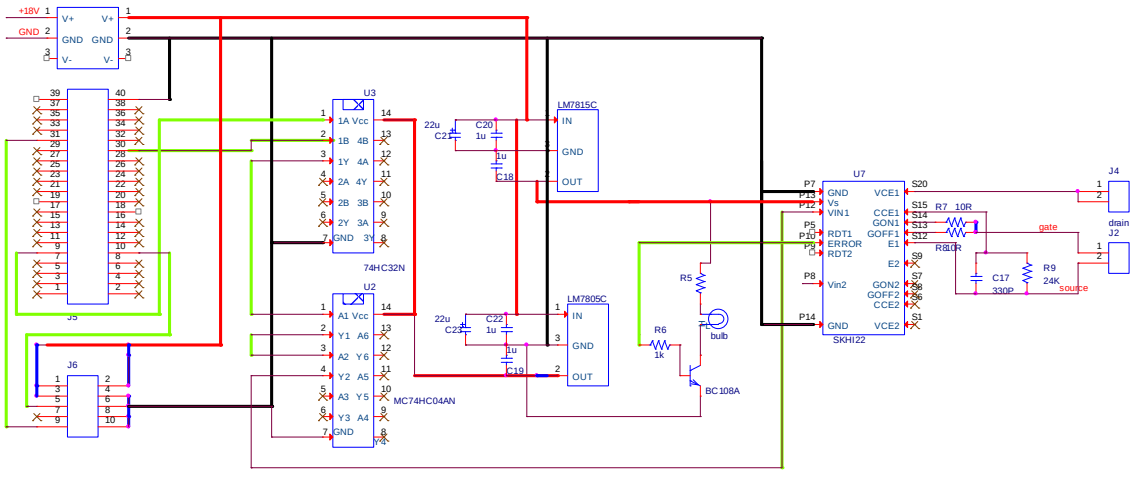


Fig. B.1 Gate driver circuits for the clamp switch of the FC converter

Appendix C

Averaging the Boost Inductor Current Waveform

The boost inductor voltage and current waveforms are shown in Fig. 3.1 and Fig. 3.7 which are sketched based on the converter operation in Fig. 3.2. During the overlap periods $\frac{d_1 T_s}{2}$ and $\frac{d_2 T_s}{2}$ (which are represented by the subintervals{(t_0 , t_1), (t_1 , t_2), (t_2 , t_3), (t_3 , t_4)} and {(t_8 , t_9), (t_9 , t_{10}), (t_{10} , t_{11}), (t_{11} , t_{12})} respectively), the voltage across the boost inductor L_b is equal to $v_{fc}(t)$. While when one pair of diagonal bridge switches is turned off (i.e. the periods $\frac{d_1' T_s}{2}$ and $\frac{d_2' T_s}{2}$ which are represented by the subintervals{(t_4 , t_5), (t_5 , t_6), (t_6 , t_7), (t_7 , t_8)} and {(t_{12} , t_{13}), (t_{13} , t_{14}), (t_{14} , t_{15}), (t_{15} , t_{16})} respectively) the voltage across the boost inductor L_b is equal to $[v_{fc}(t) - v_{Ca}(t)]$. This is can be found in the first row of the dynamic equations (4.2) and (4.4) to (4.7).

By replacing the variables v_{fc}, v_{Ca}, v_o, i_{Lb}, and $i_{L\sigma}$ in equations (4.2) and (4.4) to (4.7) with their low-frequency averaged values$\langle v_{fc}(t)\rangle_{T_s}$, $\langle v_{Ca}(t)\rangle_{T_s}$, $\langle v_o(t)\rangle_{T_s}$, $\langle i_{Lb}(t)\rangle_{T_s}$, and $\langle i_{L\sigma}(t)\rangle_{T_s}$, the low-frequency average boost inductor $\langle v_{Lb}(t)\rangle_{T_s}$over T_s can be given as:

$$
\begin{aligned}
L_b \frac{d\langle i_{Lb}(t)\rangle_{T_s}}{dt} &= \langle V_{Lb}(t)\rangle_{T_s} \\
&= \langle v_{fc}(t)\rangle_{T_s} \frac{d_1(t)}{2} + \left(\langle v_{fc}(t)\rangle_{T_s} - \langle v_{ca}(t)\rangle_{T_s}\right) \frac{d_1'(t)}{2} \\
&+ \langle v_{fc}(t)\rangle_{T_s} \frac{d_2(t)}{2} + \left(\langle v_{fc}(t)\rangle_{T_s} - \langle v_{ca}(t)\rangle_{T_s}\right) \frac{d_2'(t)}{2}
\end{aligned}
\qquad \text{(C.1)}
$$

Simplify equation (C.1), (4.8) can be obtained.

Appendix D

Full Derivation of the Control-to-Output Transfer Function $G_{vd}(s)$

This appendix shows how the $G_{vd}(s)$ was derived for the proposed converter. Other transfer functions can be obtained in the same way but for different conditions.

By setting $\hat{v}_{fc}(s) = 0$ in (4.23), the following equations can be obtained:

$$K\hat{i}_L(s) + D'\hat{v}_{Ca}(s) = V_{Ca}\hat{d}(s) \tag{D.1}$$

$$-D'\hat{i}_L(s) + m\hat{v}_{Ca}(s) - g_2\hat{v}_o(s) = g_1\hat{d}(s) \tag{D.2}$$

$$-J\hat{i}_L(s) - p_3\hat{v}_{Ca}(s) + b\hat{v}_o(s) = -p_1\hat{d}(s) \tag{D.3}$$

where

$$K = s.L_b, \qquad m = s.C_a + g_3, \qquad b = s.\frac{C}{2} + p_2 \tag{D.4}$$

From (D.1),

$$\hat{i}_L(s) = \frac{V_{Ca}}{K}\hat{d}(s) - \frac{D'}{K}\hat{v}_{Ca}(s) \tag{D.5}$$

Substitution of (D.5) in (D.2) yields

$$\left(\frac{(D')^2 + Km}{K}\right)\hat{v}_{Ca}(s) - \left(\frac{V_{Ca}D' + Kg_1}{K}\right)\hat{d}(s) = g_2\hat{v}_o(s) \tag{D.6}$$

(D.5) in (D.3) yields

$$\left(\frac{JD' - Kp_3}{K}\right)\hat{v}_{Ca}(s) = -\left(\frac{Kp_1 - JV_{Ca}}{K}\right)\hat{d}(s) - b\hat{v}_o(s) \tag{D.7}$$

By simplifying and rearranging the terms of (D.7), $\hat{v}_{Ca}(s)$ becomes:

$$\hat{v}_{Ca}(s) = \frac{JV_{Ca} - Kp_1}{JD' - Kp_3}\hat{d}(s) - \frac{bK}{JD' - Kp_3}\hat{v}_o(s) \tag{D.8}$$

Substitution of (D.8) in (D.6) gives:

$$\left(\frac{((D')^2 + Km)(JV_{Ca} - Kp_1)}{K(JD' - Kp_3)}\hat{d}(s) - \frac{bK((D')^2 + Km)}{K(JD' - Kp_3)}\hat{v}_o(s)\right) - \left(\frac{V_{Ca}D' + Kg_1}{K}\right)\hat{d}(s) = g_2\hat{v}_o(s) \tag{D.9}$$

Rearrange (D.9) into transfer function form:

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{-(D')^2p_1 + mJV_{Ca} - mKp_1 - JD'g_1 + p_3V_{Ca}D' + Kp_3g_1}{Jg_2D' - Kg_2p_3 + b(D')^2 + Kbm} \tag{D.10}$$

Substitute the coefficients in Table 4.2 and (D.4):

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{-(D')^2p_1 + (sC_a + g_3)JV_{Ca} - (sC_a + g_3)sL_bp_1 - JD'g_1 + p_3V_{Ca}D' + sL_bp_3g_1}{Jg_2D' - sLg_2p_3 + (\frac{sC + 2p_2}{2})(D')^2 + sL(\frac{sC + 2p_2}{2})(sC_a + g_3)} \tag{D.11}$$

which when written as coefficients of $\mathbf{s}$ yields

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{-(D')^2p_1 + JV_{Ca}C_a\mathbf{s} + JV_{Ca}g_3 - L_bC_ap_1\mathbf{s^2} - L_bp_1g_3\mathbf{s} - JD'g_1 + p_3V_{Ca}D' + L_bp_3g_1\mathbf{s}}{Jg_2D' - L_bg_2p_3\mathbf{s} + \frac{(D')^2C\mathbf{s}}{2} + (D')^2p_2 + \frac{L_bC_aC\mathbf{s^3}}{2} + L_bC_ap_2\mathbf{s^2} + \frac{g_3L_bC\mathbf{s^2}}{2} + g_3L_bp_2\mathbf{s}} \tag{D.12}$$

Finally:

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \left\{\frac{(p_3V_{Ca}D' + JV_{Ca}g_3 - JD'g_1 - (D')^2p_1)}{(p_2(D')^2 + Jg_2D')}\right\} \times \frac{\frac{-L_bC_ap_1}{(p_3V_{Ca}D' + JV_{Ca}g_3 - JD'g_1 - (D')^2p_1)}\mathbf{s^2} + \frac{(JV_{Ca}C_a - L_bp_1g_3 + L_bp_3g_1)}{(p_3V_{Ca}D' + JV_{Ca}g_3 - JD'g_1 - (D')^2p_1)}\mathbf{s} + 1}{\frac{L_bCC_a}{2}}{(p_2(D')^2 + Jg_2D')}\mathbf{s^3} + \frac{(L_bC_ap_2 + \frac{g_3L_bC}{2})}{(p_2(D')^2 + Jg_2D')}\mathbf{s^2} + \frac{(g_3L_bp_2 - L_bg_2p_3 + \frac{(D')^2C}{2})}{(p_2(D')^2 + Jg_2D')}\mathbf{s} + 1} \tag{D.13}$$

Then (4.24) is obtained as shown in Chapter 4.

Appendix E

Elimination of the Fraction Period Duty Cycle $\hat{\delta}(t)$ from State-Space Equation (4.21)

An elimination of the superimposed small AC variation of the fraction period duty cycle $\hat{\delta}(t)$ from the state–space equation (4.21) can be obtained as follows:

Since there is no net change in $i_{L\sigma}$ over T_s, the average leakage inductor voltage state is equal to zero, thus:

$$\langle v_{L\sigma}(t)\rangle_{T_s} = \left(\langle v_{ca}(t)\rangle_{T_s} - \frac{\langle v_o(t)\rangle_{T_s}}{2n}\right)\frac{d_1'(t)}{2} - \left(\frac{\langle v_o(t)\rangle_{T_s}}{2n}\right)\frac{\delta_2(t)}{2} + \left(\langle v_{ca}(t)\rangle_{T_s} - \frac{\langle v_o(t)\rangle_{T_s}}{2n}\right)\frac{d_2'(t)}{2} - \left(\frac{\langle v_o(t)\rangle_{T_s}}{2n}\right)\frac{\delta_1(t)}{2} = 0 \tag{E.1}$$

Using (4.10) and (4.18), (E.1) can be rewritten as:

$$\left(\langle v_{ca}(t)\rangle_{T_s} - \frac{\langle v_o(t)\rangle_{T_s}}{2n}\right)d'(t) = \left(\frac{\langle v_o(t)\rangle_{T_s}}{2n}\right)\delta(t) \tag{E.2}$$

Using small signal approximation on the non-linear equation (E.2), the following expression can be obtained:

$$\left(V_{ca} + \hat{v}_{ca}(t) - \frac{V_o + \hat{v}_o(t)}{2n}\right)\left(D' - \hat{d}(t)\right) = \left(\frac{V_o + \hat{v}_o(t)}{2n}\right)\left(\Delta + \hat{\delta}(t)\right) \tag{E.3}$$

By neglecting DC quantities and nonlinear AC terms, equation (4.22) can be obtained.

Appendix F

Matlab Code for the Transfer Function Gvd(s) of Config.2, Config.3 and Proposed Configuration.

```
Note: D1=D',D11=Δ, LK=Lσ, IL=ILb
%%%%%Config.2%%%

G1go=Vo*(D2)^-1;
m3=(-n*L*IL)*(Vo*D2)^-1;
q4=(n^2*L*C)*(2*D2^2)^-1;
q5=(n^2*L)*(D2^2*Ro)^-1;
G1vd = tf([m3 1],[q4 q5 1]);

pzmap(G1vd*G1go)

hold on

%%%%%Config.3%%%

g1=((D1*(2*LK*fs)^-1)*(Vca-Vo*(n)^-1))-IL;
g2=((D1)^2)*(2*n*LK*fs)^-1;
D11=((Vca-(Vo/(2*n)))/(Vo/(2*n)))*D1;
J=((D1+D11))*n^-1;
g3=((D1)^2)*(2*LK*fs)^-1;
p1=(IL*Vca)*(Vo)^-1;
p2=((J*IL)*(Vo)^-1)+(Ro)^-1;
p3=(IL*D1)*(Vo)^-1;
Ggo=(-p1*(D1)^2+J*g3*Vca-J*D1*g1+p3*Vca*D1)*(p2*(D1)^2+J*g2*D1)^-1;
m1=(-L*Ca*p1)*(-p1*(D1)^2+J*g3*Vca-J*D1*g1+p3*Vca*D1)^-1;
m2=(Ca*J*Vca-g3*p1*L+p3*g1*L)*(-p1*(D1)^2+J*g3*Vca-
J*D1*g1+p3*Vca*D1)^-1;
q1=(L*C*Ca)*(2*p2*(D1)^2+2*J*g2*D1)^-1;
q2=(L*C*g3+2*Ca*L*p2)*(2*p2*(D1)^2+2*J*g2*D1)^-1;
q3=(C*(D1)^2-2*g2*p3*L+2*p2*g3*L)*(2*p2*(D1)^2+2*J*g2*D1)^-1;
Gvd = tf([m1 m2 1],[q1 q2 q3 1]);

pzmap(Gvd*Ggo)

%%%%%proposed%%%

g1=((D1*(LK*fs)^-1)*(Vca-Vo*(2*n)^-1))-IL;
g2=((D1)^2)*(4*n*LK*fs)^-1;
D11=((Vca-(Vo/(n)))/(Vo/(n)))*D1;
J=((D1+D11))*n^-1;
g3=((D1)^2)*(2*LK*fs)^-1;
p1=(2*IL*Vca)*(Vo)^-1;
p2=((J*IL)*(Vo)^-1)+(Ro)^-1;
p3=(2*IL*D1)*(Vo)^-1;
Ggo=(-p1*(D1)^2+J*g3*Vca-J*D1*g1+p3*Vca*D1)*(p2*(D1)^2+J*g2*D1)^-1;
m1=(-L*Ca*p1)*(-p1*(D1)^2+J*g3*Vca-J*D1*g1+p3*Vca*D1)^-1;
m2=(Ca*J*Vca-g3*p1*L+p3*g1*L)*(-p1*(D1)^2+J*g3*Vca-
J*D1*g1+p3*Vca*D1)^-1;
```

```
q1=(L*C*Ca)*(2*p2*(D1)^2+2*J*g2*D1)^-1;
q2=(L*C*g3+2*Ca*L*p2)*(2*p2*(D1)^2+2*J*g2*D1)^-1;
q3=(C*(D1)^2-2*g2*p3*L+2*p2*g3*L)*(2*p2*(D1)^2+2*J*g2*D1)^-1;
Gvd = tf([m1 m2 1],[q1 q2 q3 1]);
pzmap(Gvd*Ggo)
```

Appendix G

PSpice and Simulink Circuit Diagrams for the CFC

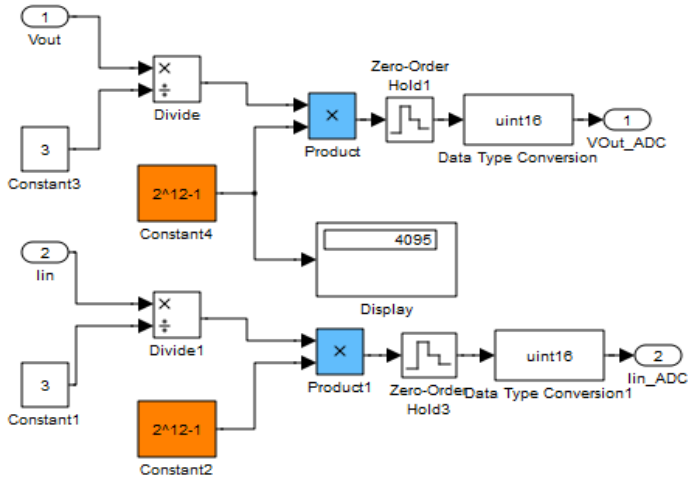


Fig. G.1 On-chip ADC emulator

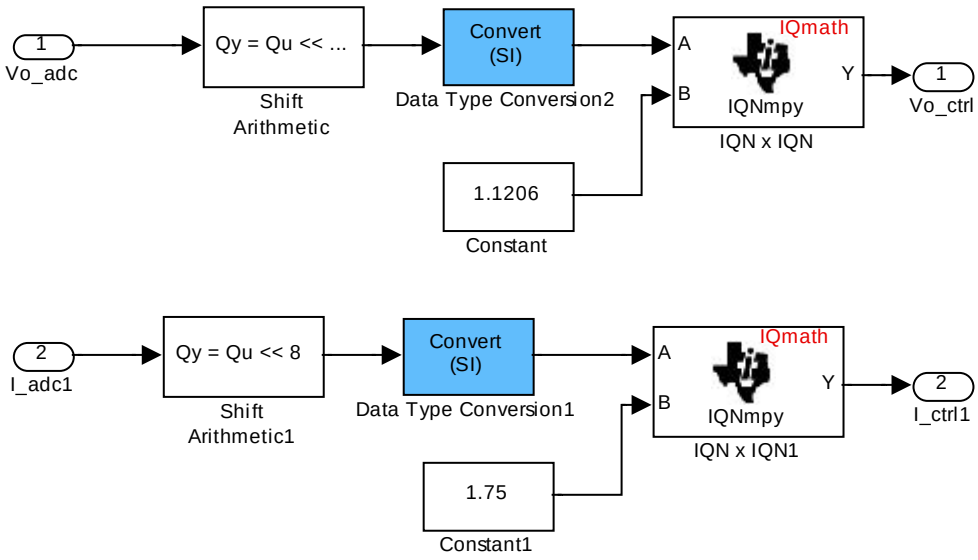


Fig. G.2 Data-scale unit for the measured signals

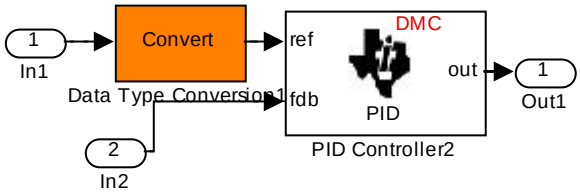


Fig. G.3 PID controller provided by th TI library

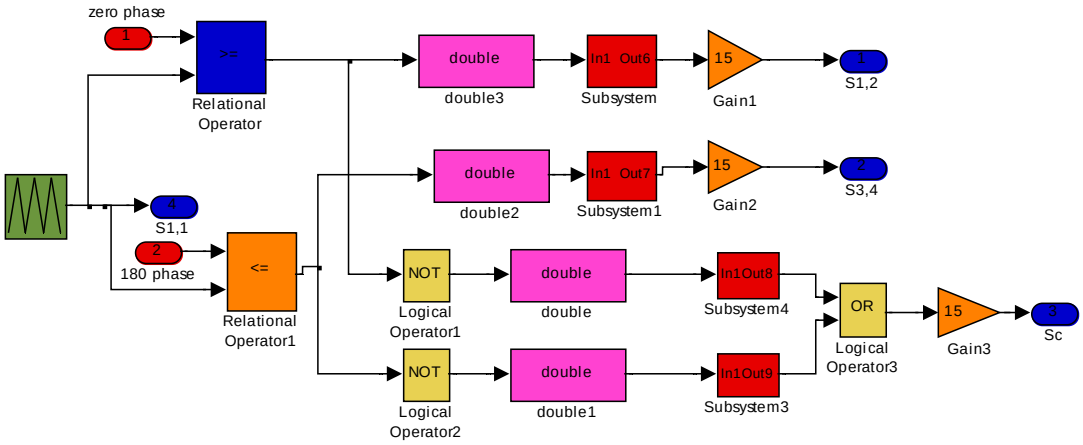


Fig. G.4 PWM block digram

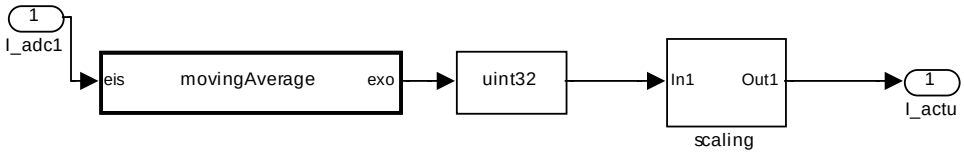


Fig. G.5 ADC_ scaling block of Fig. 4.25

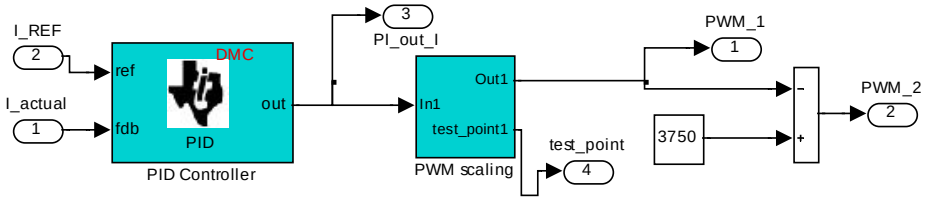


Fig. G.6 PI controller block of Fig. 4.25

Appendix H

Overlap PWM Generation for the FBCFC

An open-loop test on the FC converter was carried out to measure the converter's efficiency, FC current, output current, and the input and output power (see results of Chapter 3). This was done by controlling the required duty cycle in respect to the output power changes as described below.

As shown in Fig. 3.1, the proposed converter requires three PWM signals within the same switching period T_s. The gate signals of the diagonal main switches should overlap each other by a period equal to a half of the duty cycle D. Furthermore, the gate signal of the clamp switch should be delayed from the main switching devices at the lagging and leading edges by a period equal to the resonant period of the leakage inductance and parasitic capacitance of the main and clamp switches. To implement the above PWM in a DSP, one could employ two independent general purpose timers (GPxT) to synchronize two counters (T1CNT and T2CNT) of the Event Managers (EVA and EVB) with 180^0 phase shift. This means more GP timers are required when further PWM outputs are needed. However, the number of timers in a selected DSP is limited to four. Therefore, the PWM signals for all switches are generated using only one GP timer with a dead-band zone[1]. By setting the GP timer (T1) in continuous up-down counting mode to generate a symmetrical PWM for the main switches, one can update the value in the Compare Registers in such a way that D goes to minimum value when CMPR1 is half of the time period (T1PR) and ACTR register set to active high, while the CMPR2 (= T1PR-CMPR1) and ACTR register set to active low. To set D for

[1] Using this method, a single DSP processor can be used to generate PWM for both the FBCFC and the BDC described in Chapter 6.

the desired maximum value, CMPR1 should be equal to 0.725 of T1PR and CMPR2 remains equal to T1PR-CMPR1, as shown in Fig. H.1[2].

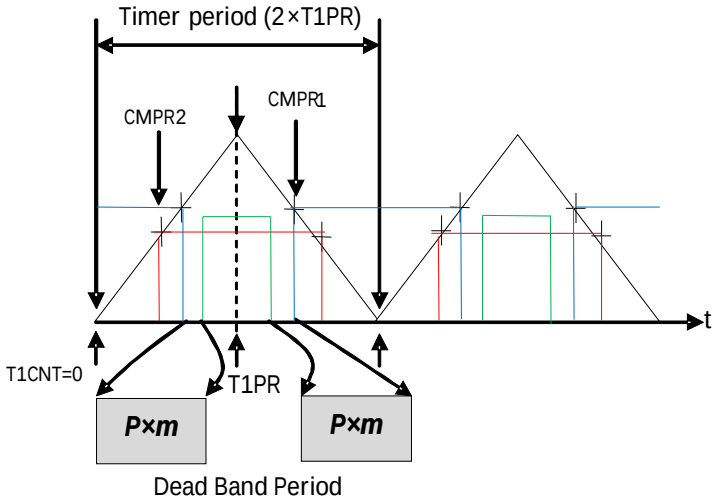


Fig. H.1 DSP-based overlap PWM with dead band

Using the same GP timer T1, the PWM with dead time for the clamp switch is generated by taking the complementary of PWM2 and PWM3 and then controlling the dead zone directly by setting the DPTCONx Register in such a way that the value (m) of that Register is set to 9 and the pre-scaler value (p) of DBTCONx is set to 8. This setting gives a 1.8μsec dead time (dead band value = p×m clock cycle) between the main and clamp switches. The above configuration was implemented using Embedded IDE software, by using one of the C281xPWM blocks with two PWM outputs (PWM1/PWM2 and PWM3/PWM4), as shown in Fig. H.2.

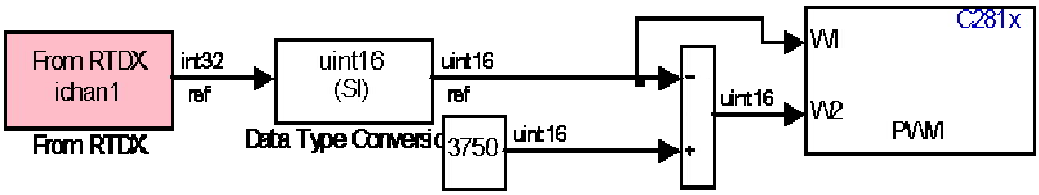


Fig. H.2 Simulink block of the overlap PWM algorithm

[2] For clarity, different amplitudes are shown for these PWM signals; in reality the levels are the same.

To control the required duty cycle in respect to full output power variations, a GUI consisting of slide bar and voltage and current measurements has been built. By setting the duty cycle with respect to the slide bar, the data is transferred from the host to the target using “From RTDX” block as shown in Fig. H.2. RTDX is a Real Time Data Exchange feature provided by TI has been utilised to provide a continuous observation in real time of the designed controller [157].

Appendix I

Example Shows How the "Mathematica" Software Tool are Used to Drive the Equations in Chapter 5 and 6

(*RMS current for the BDC under CPC when $2nV_{uc}=V_o$*)

(*for $0<\theta<\varphi$*)

In[2]:= $I_{(\theta)} == \left(\frac{V_o}{\omega L_t n} * \theta\right) + I_{t0}$

Out[2]= $I_\theta == \frac{\theta V_o}{n \omega L_t} + I_{t0}$

(*for $\varphi<\theta<\pi$*)

Out[9]= $I_\theta == -I_0 == \frac{\varphi V_o}{2 L n \omega}$

(*for $\pi<\theta<\pi+\varphi$*)

In[3]:= $I_{(\theta)} == \left(-\frac{V_o}{\omega L_t n} * (\theta - \pi)\right) + I_\pi$

Out[3]= $I_\theta == -\frac{(-\pi + \theta) V_o}{n \omega L_t} + I_\pi$

(*where*)

Out[6]= $I_0 == -\frac{\varphi V_o}{2 n \omega L_t}$

Out[7]= $I_\pi == -I_0 == \frac{\varphi V_o}{2 n \omega L_t}$

(*for $\pi+\varphi<\theta<2\pi$*)

Out[8]= $I_\theta == I_0 == -\frac{\phi V_o}{2 L n \omega}$

(*Hence, RMS primary current for over full cycle is*)

In[13]:=
$$\text{Irms} == \sqrt{\left(\frac{1}{2\pi}\left(\int_0^{\varphi}\left(\frac{(2\theta-\varphi)\,V_o}{2\,n\,\omega\,L_t}\right)^2 d\theta + \int_{\varphi}^{\pi}\left(\frac{\varphi\,V_o}{2\,n\,\omega\,L_t}\right)^2 d\theta + \int_{\pi}^{\pi+\varphi}\left(\frac{V_o}{2\,n\,\omega\,L_t}(2\pi-2\theta+\varphi)\right)^2 d\theta + \int_{\pi+\varphi}^{2\pi}\left(-\frac{\varphi\,V_o}{2\,n\,\omega\,L_t}\right)^2 d\theta\right)\right)}$$

Out[13]=
$$\text{Irms} == \frac{\sqrt{\frac{(\pi-\varphi)\,\varphi^2\,V_o^2}{2\,n^2\,\omega^2\,L_t^2} + \frac{\varphi^3\,V_o^2}{6\,n^2\,\omega^2\,L_t^2}}}{\sqrt{2\pi}}$$

In[20]:=
$$\text{Simplify}\left[\text{Irms} == \frac{\sqrt{\frac{(\pi-\varphi)\,\varphi^2\,V_o^2}{2\,n^2\,\omega^2\,L_t^2} + \frac{\varphi^3\,V_o^2}{6\,n^2\,\omega^2\,L_t^2}}}{\sqrt{2\pi}}\right]$$

Out[20]=
$$\text{Irms} == \frac{\sqrt{\frac{(3\pi-2\varphi)\,\varphi^2\,V_o^2}{n^2\,\omega^2\,L_t^2}}}{2\sqrt{3\pi}}$$

(*from the Power equation of the BDC under CPC, the required L_t can be obtained as*)

$$P_{uc} == \frac{(\pi-\varphi)\,\varphi\,V_o\,V_{uc}}{2\,n\,\pi\,\omega\,L_t}$$

In[19]:=
$$\text{Solve}\left[P_{uc} == \frac{(\pi-\varphi)\,\varphi\,V_o\,V_{uc}}{2\,n\,\pi\,\omega\,L_t},\ L_t\right]$$

Out[19]=
$$\left\{\left\{L_t \to \frac{(\pi-\varphi)\,\varphi\,V_o\,V_{uc}}{2\,n\,\pi\,\omega\,P_{uc}}\right\}\right\}$$

(*Subtitute L_t in Out[20]*)

In[23]:=
$$\text{Simplify}\left[\text{Irms} == \frac{\sqrt{\frac{(3\pi-2\varphi)\,\varphi^2\,V_o^2}{n^2\,\omega^2\,L_t^2}}}{2\sqrt{3\pi}},\ L_t = \frac{(\pi-\varphi)\,\varphi\,V_o\,V_{uc}}{2\,n\,\pi\,\omega\,P_{uc}}\right]$$

Out[23]=
$$\sqrt{3\pi}\sqrt{\frac{(3\pi-2\varphi)\,P_{uc}^2}{(\pi-\varphi)^2\,V_{uc}^2}} == 3\,\text{Irms}$$

In[24]:=
$$\text{Solve}\left[\sqrt{3\pi}\sqrt{\frac{(3\pi-2\varphi)\,P_{uc}^2}{(\pi-\varphi)^2\,V_{uc}^2}} == 3\,\text{Irms},\ \text{Irms}\right]$$

Appendix J

Average Power and Phase-Shift Angles Values that have been Used for Different Operating Modes

TABLE J.1
FOR V_{UC} = 48V

Power P_{uc}	Mode I $0^0 \le \varphi_1 \le 90^0$ $0^0 \le \varphi_2 \le 90^0$		Mode II $0^0 \le \varphi_1 \le 90^0$ $0^0 \le \varphi_2 \le 90^0$		Mode III $90^0 \le \varphi_1 \le 180^0$ $90^0 \le \varphi_2 \le 180^0$		Mode IV $90^0 \le \varphi_1 \le 180^0$ $0^0 \le \varphi_2 \le 90^0$		Mode V $0^0 \le \varphi_1 \le 90^0$ $90^0 \le \varphi_2 \le 180^0$	
	$\varphi_1=\varphi_2$	φ_2	$\varphi_1 \le \varphi_2/2$	φ_2	φ_1	φ_2	φ_1	φ_2	$\varphi_1 \le \varphi_2/2$	φ_2
112	φ_2	8	2	8	124	97	104	73	3	178
225	φ_2	17	6	16	124	103	104	79	6	176
346	φ_2	28	7	26	124	110	99	88	8	170
440	φ_2	38	7	34	126	118	101	88	9	162
535	φ_2	51	8	54	127	126	97	89	9	154
603	φ_2	64	9	52	122	124	92	89	15	161
659	φ_2	90	6	69	120	127	90	90	7	132

TABLE J.2
FOR V_{UC} = 44V

Power P_{uc}	Mode I $0^0 \le \varphi_1 \le 90^0$ $0^0 \le \varphi_2 \le 90^0$		Mode II $0^0 \le \varphi_1 \le 90^0$ $0^0 \le \varphi_2 \le 90^0$		Mode III $90^0 \le \varphi_1 \le 180^0$ $90^0 \le \varphi_2 \le 180^0$		Mode IV $90^0 \le \varphi_1 \le 180^0$ $0^0 \le \varphi_2 \le 90^0$		Mode V $0^0 \le \varphi_1 \le 90^0$ $90^0 \le \varphi_2 \le 180^0$	
	$\varphi_1=\varphi_2$	φ_2	$\varphi_1 \le \varphi_2/2$	φ_2	φ_1	φ_2	φ_1	φ_2	$\varphi_1 \le \varphi_2/2$	φ_2
103	φ_2	8	2	8	124	97	104	73	3	178
207	φ_2	17	6	16	124	103	104	79	6	176
318	φ_2	28	7	26	124	110	99	80	8	170
403	φ_2	38	7	34	126	118	101	88	9	162
491	φ_2	51	8	54	127	126	97	89	9	154
554	φ_2	64	9	60	122	124	92	89	15	161
604	φ_2	90	6	69	120	127	90	90	7	132

TABLE J.3
FOR V_{UC} = 28V

Power P_{uc}	Mode I $0^0 \le \varphi_1 \le 90^0$ $0^0 \le \varphi_2 \le 90^0$		Mode II $0^0 \le \varphi_1 \le 90^0$ $0^0 \le \varphi_2 \le 90^0$		Mode III $90^0 \le \varphi_1 \le 180^0$ $90^0 \le \varphi_2 \le 180^0$		Mode IV $90^0 \le \varphi_1 \le 180^0$ $0^0 \le \varphi_2 \le 90^0$		Mode V $0^0 \le \varphi_1 \le 90^0$ $90^0 \le \varphi_2 \le 180^0$	
	$\varphi_1=\varphi_2$	φ_2	$\varphi_1 \le \varphi_2/2$	φ_2	φ_1	φ_2	φ_1	φ_2	$\varphi_1 \le \varphi_2/2$	φ_2
66	φ_2	8	2	8	124	97	104	73	3	178
132	φ_2	17	6	16	124	103	104	79	6	176
202	φ_2	28	7	26	124	110	99	81	8	170
256	φ_2	38	7	34	126	118	101	88	9	162
312	φ_2	51	8	44	127	126	97	89	9	154
352	φ_2	64	9	52	122	124	92	89	15	161
384	φ_2	90	6	69	120	127	90	90	7	132

Appendix K

PSpice and Simulink Circuit Diagrams for the BDC

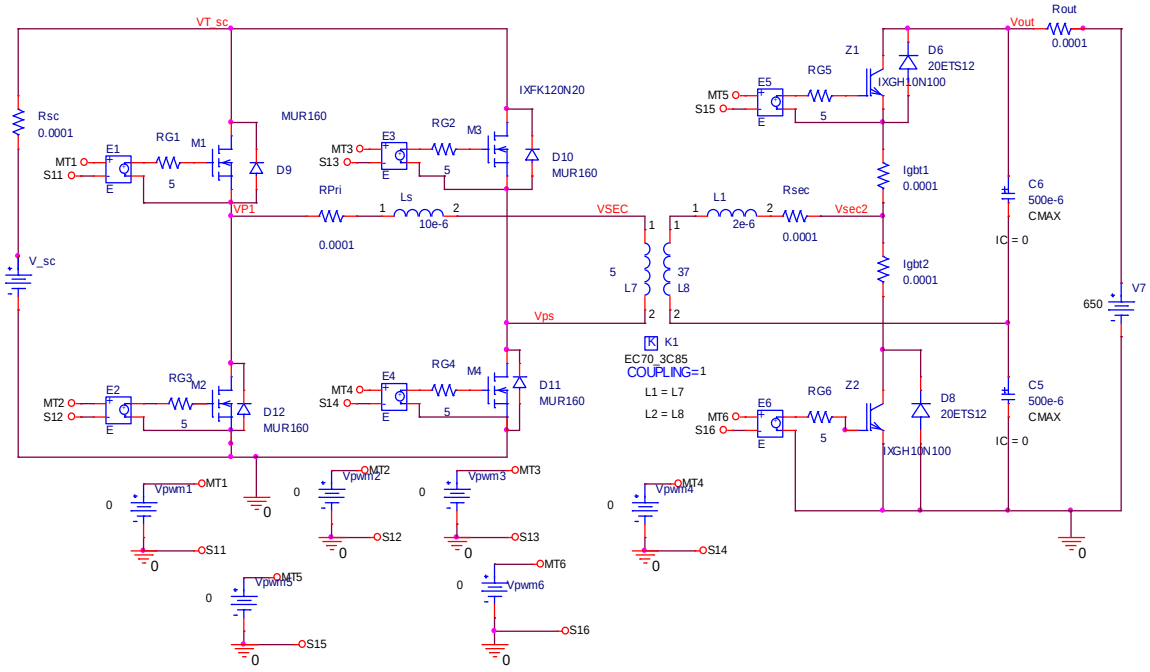
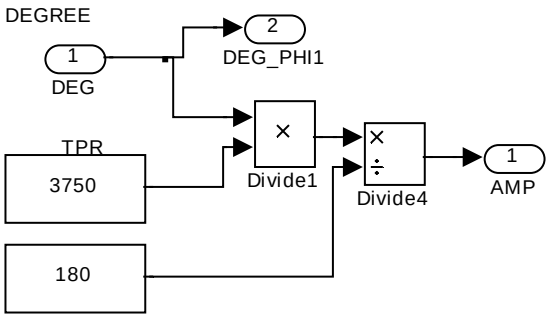


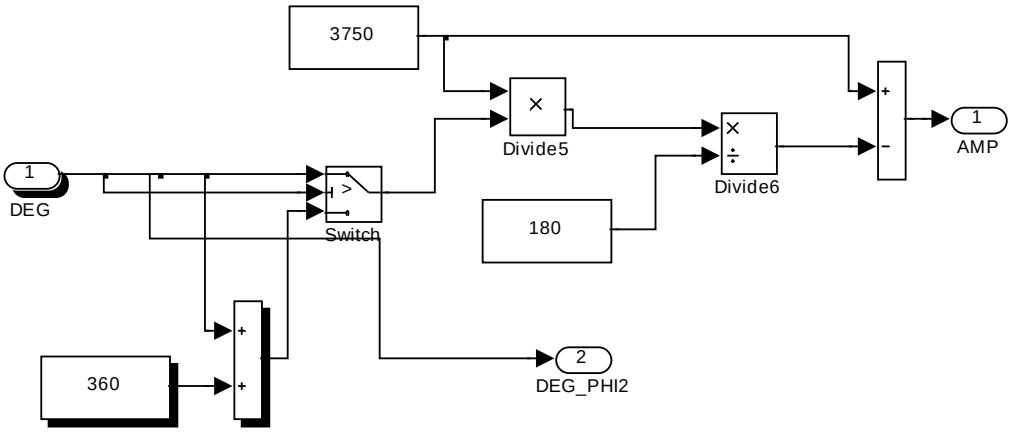
Fig. K.1 PSpice schematic circuit diagram of the BDC with voltage-doubler circuit (Vpwm1, Vpwm2, Vpwm3, Vpwm4, Vpwm5, Vpwm6 and V_SC are indicating the PWM and UC voltage signals supplied from Matlab to the PSpice circuit via SLPS software. VT_sc, VP1, VSEC, Vps, IRsc, Vsec2, Vout, Igbt1and Igbt2 are the measurement signals sent by PSpice to the Simulink model in Fig. 5.36 via the SLPS software.

Before generating the required PWM signals for each switching device the output of the embedded function is connected to the PWM scaling blocks in order to convert the phase-shift angles in degree to the amplitude values (see blocks “Deg. to Amp.” in Fig. 6.27), where the details of the block is depicted in Fig. K.2a and b. This is required in order to implement the novel optimal modulation scheme on the same 32-bit fixed-point DSP processor described in Section 4.6.2. After the phase-shift angles are scaled the

output of the blocks “Deg. to Amp.” are connected to the PWM module to generate the required PWM with fixed 50% duty cycle and two phase-shift angles.



(a)



(b)

Fig. K.2 Detailed block diagram of the “Deg To Amp” blocks in Fig. 6.27
(a) conversion for phase-shift φ_1 (b) conversion for phase-shift φ_2

Fig. K.3 demonstrates the implementation method to produce the required PWM signals for the BDC switches with two phase-shift angles and fixed 50% duty cycle using one timer. As can be seen the PWM7 for the switch S1 selected as the reference for the PWM9 and PWM11 of the switches S3 and Z1 respectively. This is achieved by comparing the half of the timer period (0.5T2PR1) with the carrier signal (TRI), which

[1] Notice that T2PR is a period register to adjust the required switching time of the carrier signal associated with the GP Timer T2. For example, to generate 20 kHz (50μsec) PWM signal, the amplitude

is set in continuous up-down counting mode (block “GPT2”), and kept the control signal CTR1 constant. The amplitude of the phase-shift PS1 and PS2 are added and subtracted from 0.5T2PR as indicated in the blocks “CMPR1” and “CMPR2” in Fig. 6.27b (see Fig. K.4 for the block detail). The outputs of these blocks are compared with the derivative of TRI (see Fig. K.5) to generate the control signals CTR2 and CTR3 for the PWM modules 2 and 3 respectively in Fig. 6.27. PWM modules 1, 2 and 3 are identical and shown in Fig. K.6. The same arrangement above can be achieved in the DSP just by programming the event manager EVB so that updating the compare registers CMPR3 and CMPR4 using the ISR with the phase-shift values PS1 and PS2 every half cycle. Using this method the same DSP can be used to control both the FC converter and the UC converter by using only two GP timers T1 and T2. This arrangement illustrated in Fig. K.7.

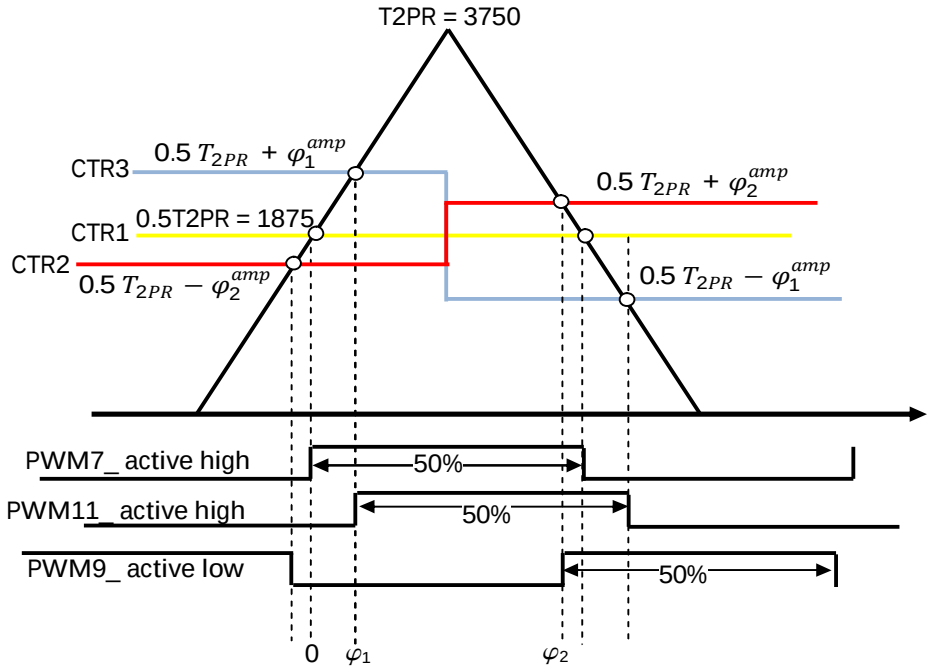


Fig. K.3 Fixed 50% duty cycle PWM implementation for the BDC with voltage-doubler (φ_1^{amp} and φ_2^{amp} are amplitude value of the phase shift angles φ_1 and φ_2 equal to PS1 and PS2 in Fig. 6.27)

of the carrier signal is calculating as (switching time ×HSPCLK), where HSPCLK is the high speed peripheral clock of the processor presale as 75MHz gives carrier signal amplitude equal to 3750.

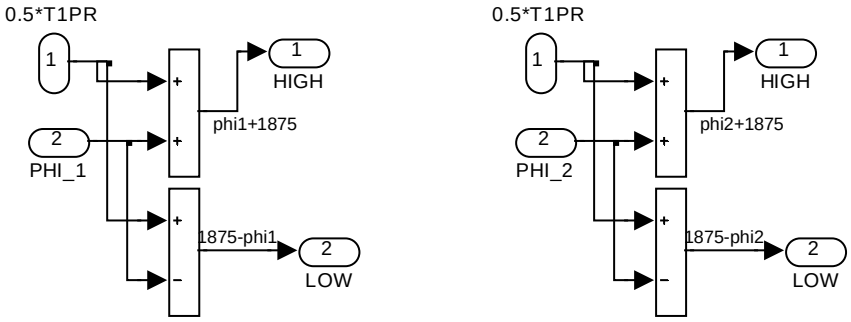


Fig. K.4 Detailed block diagram of the blocks “CMPR3” and “CMPR4” in Fig. 5.36b

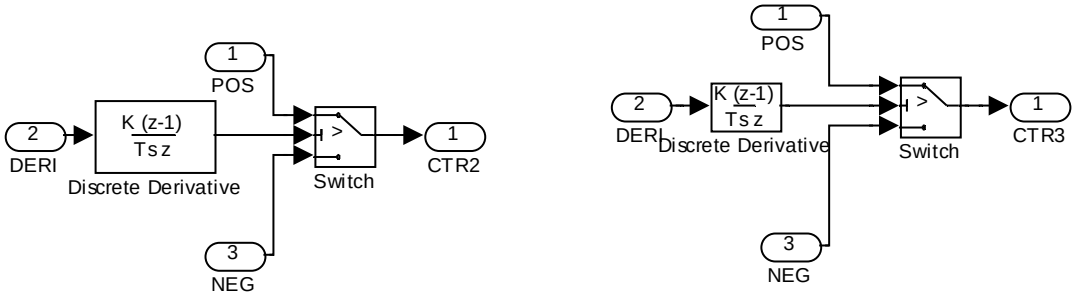


Fig. K.5 Detailed block diagram of the blocks “Dervi_1” and “Dervi2” in Fig. 5.36b

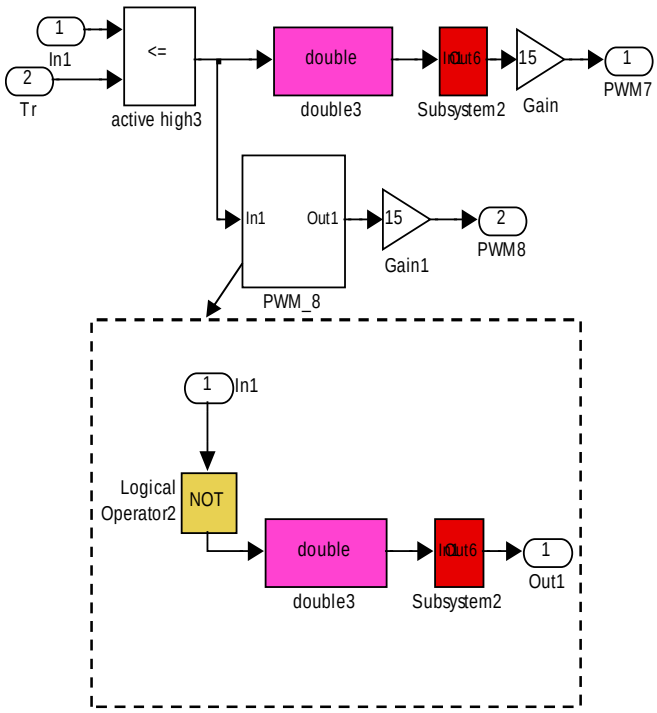


Fig. K.6 Detailed block diagram of the PWM modules

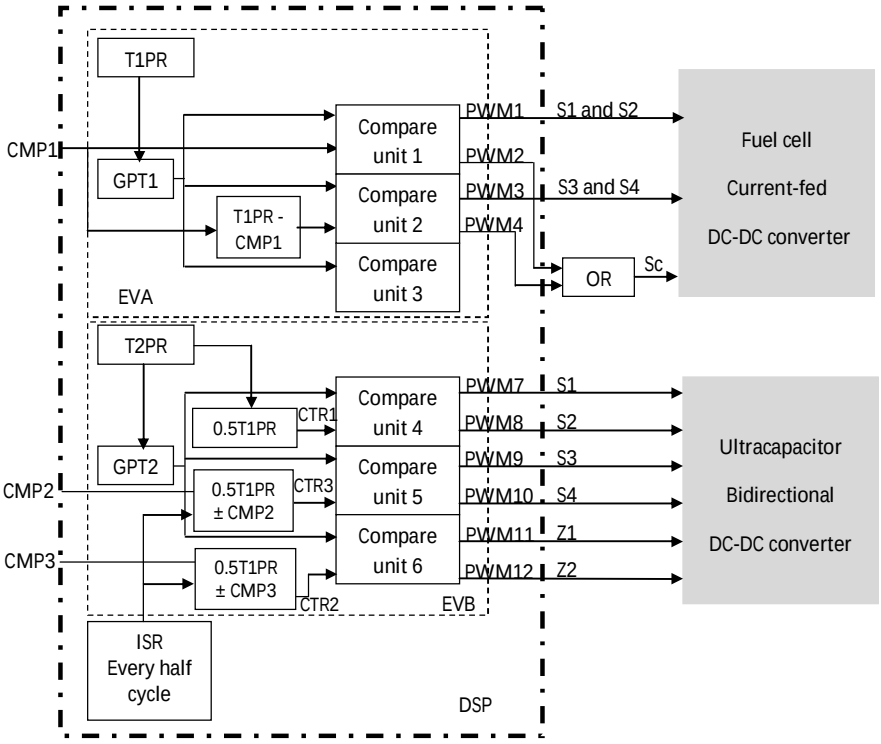


Fig. K.7 Block diagrams for controlling the FC and UC converters with one DSP processor. Notice that CMP2 is the Compare value equal to PS1 and CMP3 is the Compare value equal to PS2

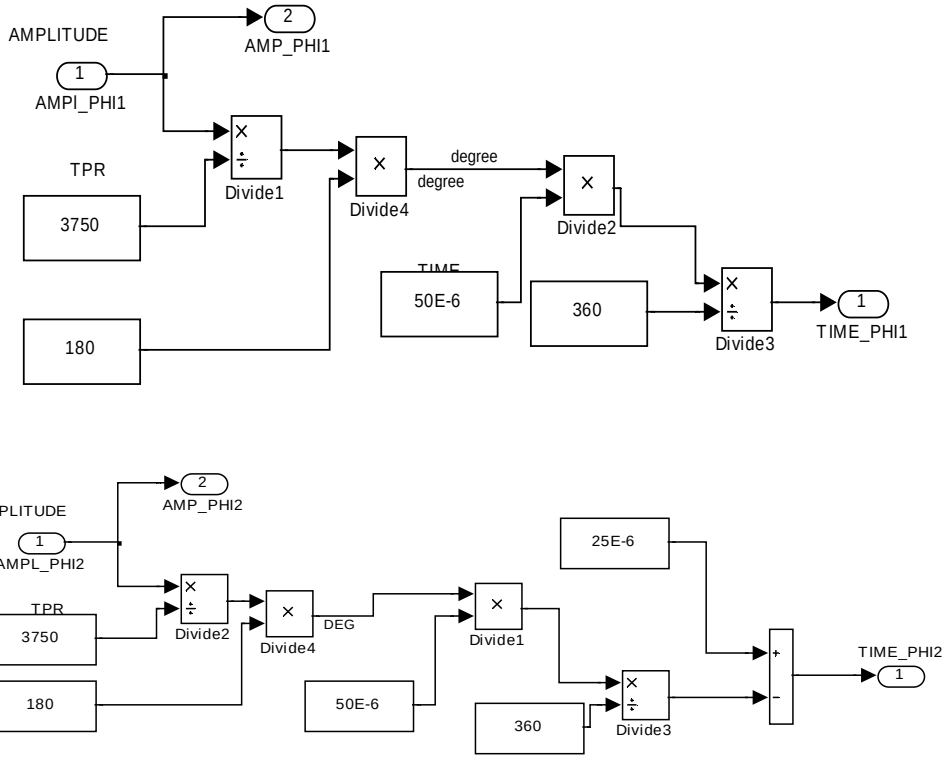
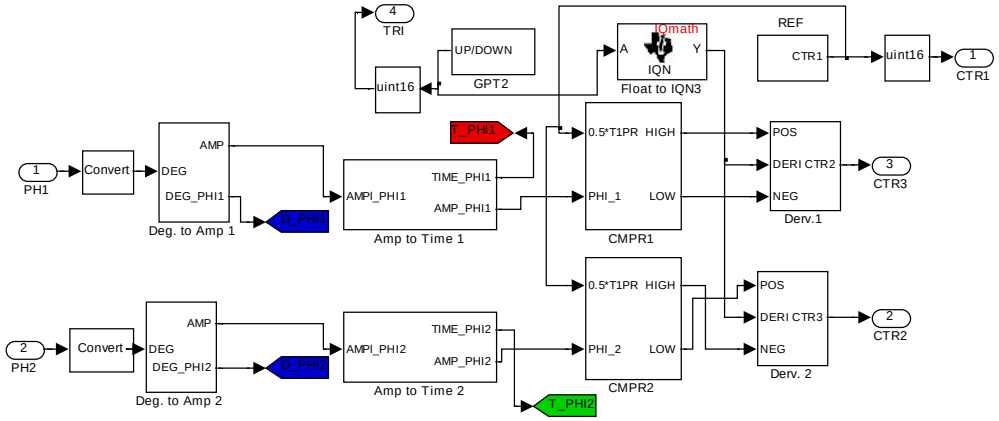
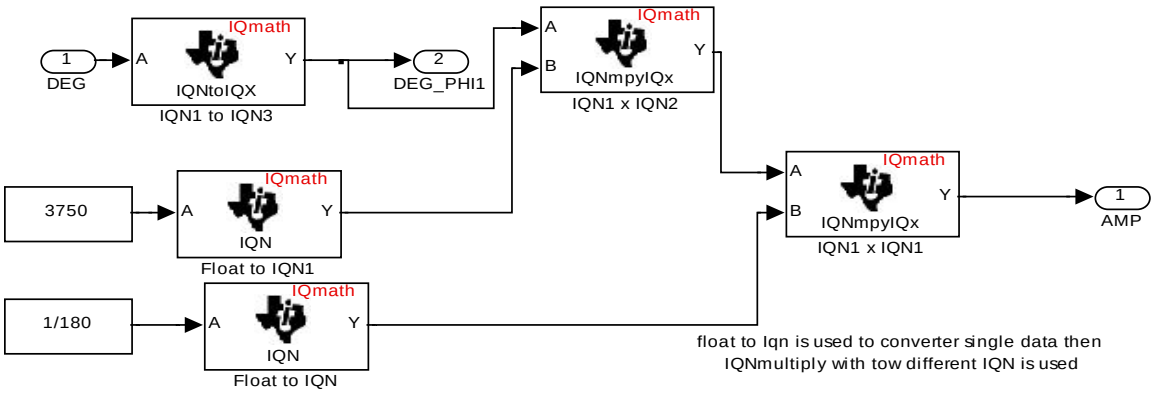


Fig. K.8 Detailed block diagram of the blocks “Amp. To Time” in Fig. 5.36b. These blocks are used to convert the amplitude values of the phase-shift angles to time form.

The following Simulink blocks are used to generate the required the PWM signals when the BDC is simulated using SLPS-PIL dual co-simulation.

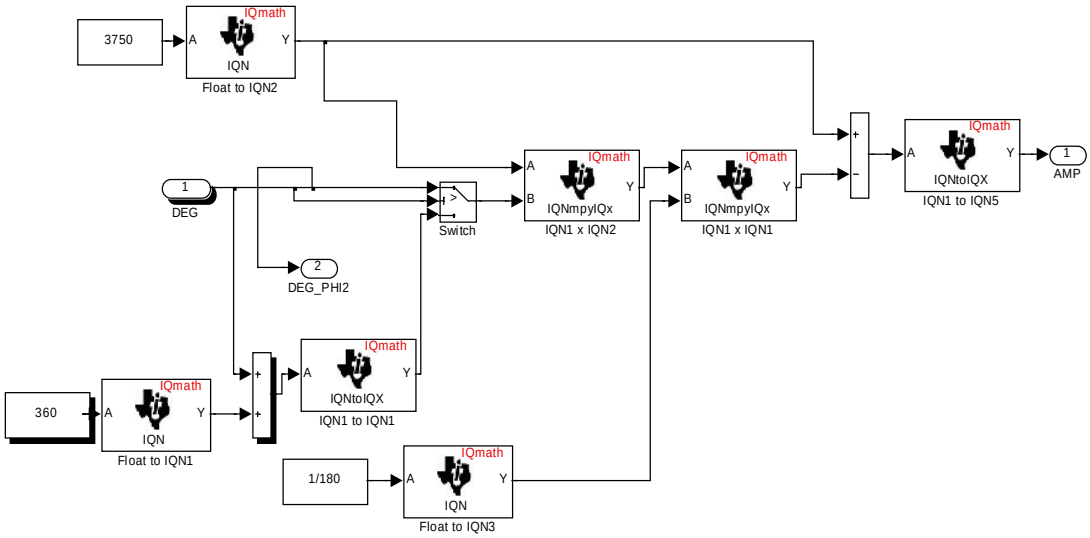


(a)

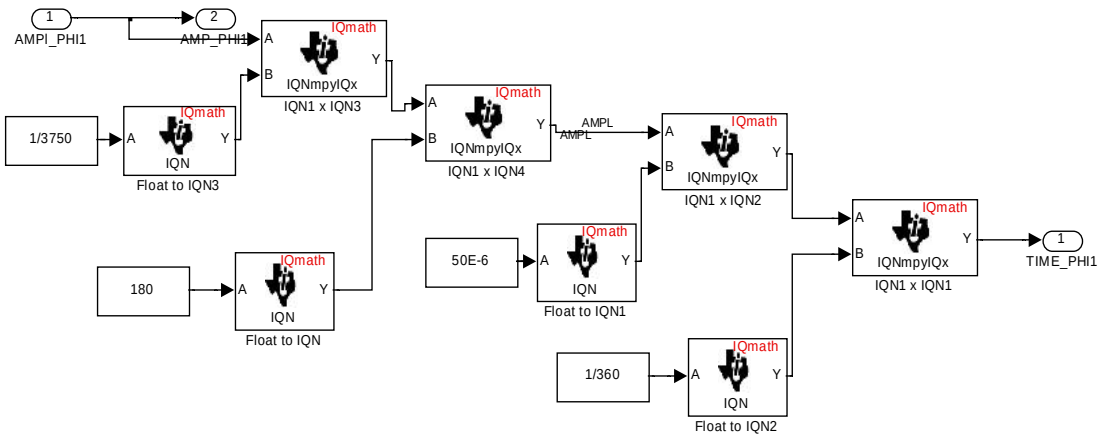


(b)

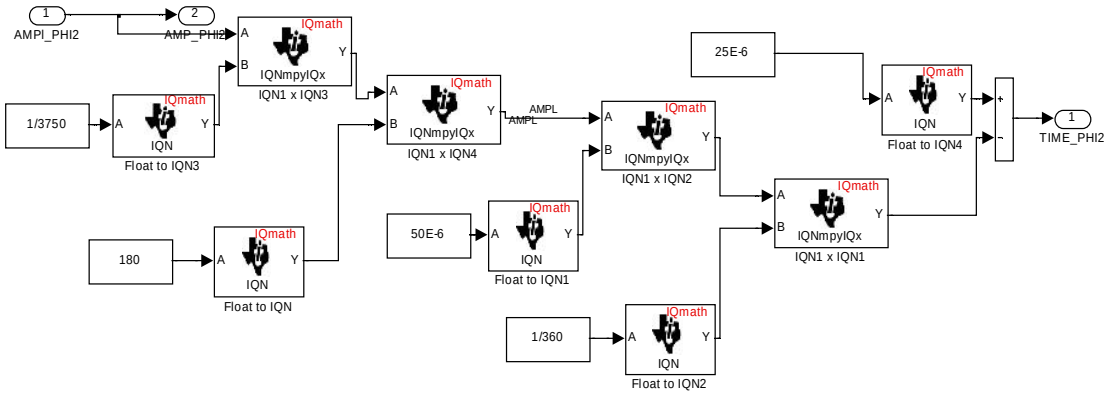
(continued in the next page)



(c)



(d)



(e)

Fig. K.9cont. Detailed block diagram of (a) the PWM circuit which is used for the SLSP-PIL dual co-simulation (b) and (c) blocks “Deg. To Amp.” used in (a). (d) and (e) blocks “Amp to Time” used in (a)

Appendix L

Schematic Diagrams of the BDC, Switch Driver Circuits, and DSP–PWM Interfacing Circuit

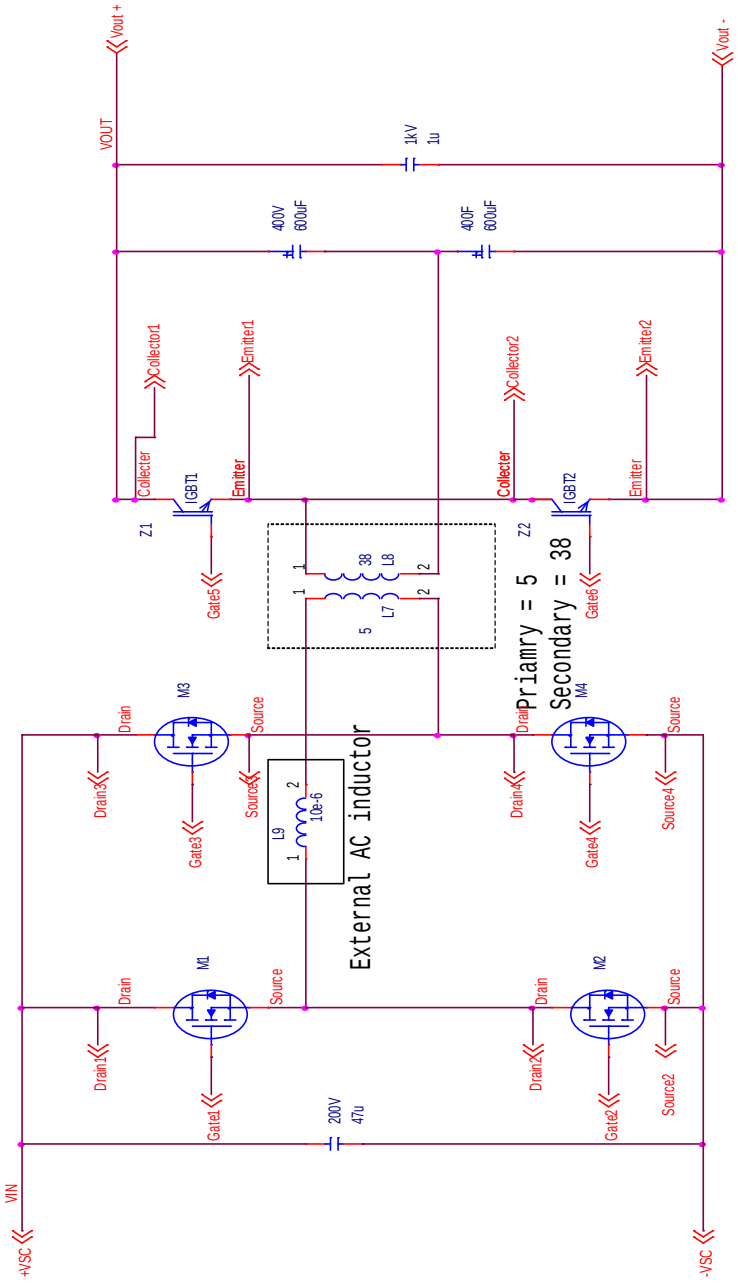


Fig. L.1 Schematic circuit diagram of the H-bridge bidirectional DC-DC converter with IGBT voltage-doubler circuit. The converter has been designed for P_{max} = 1.5KW, Input voltage = 28-48V, Output voltage = 650V, Peak input current= 80A, Peak output current 8A (IRFP4110PBF MOSFET rating = 120 A, 100V R_{on}= 3.7mΩ, IGBT rating = 1200V, 50A)

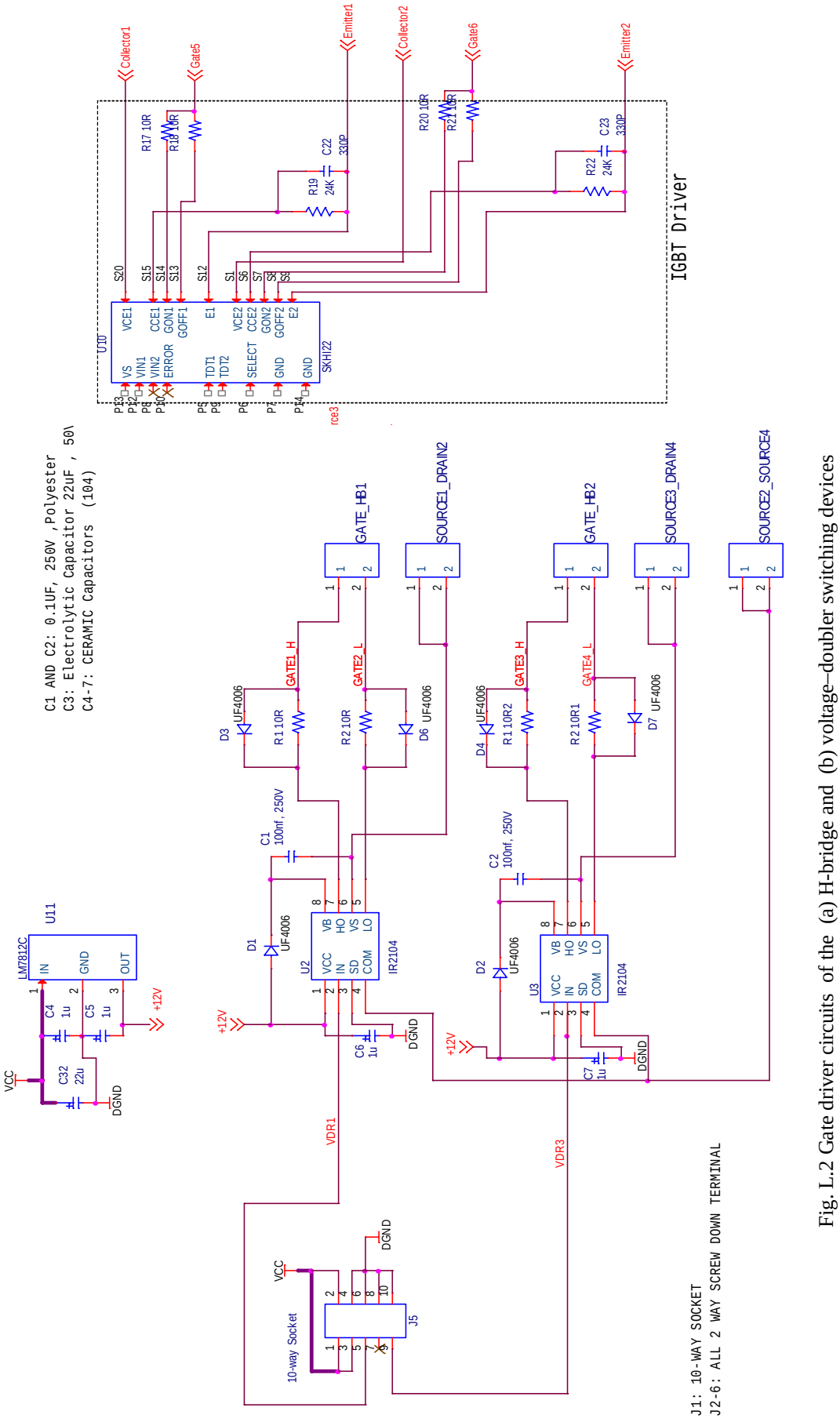


Fig. L.2 Gate driver circuits of the (a) H-bridge and (b) voltage–doubler switching devices

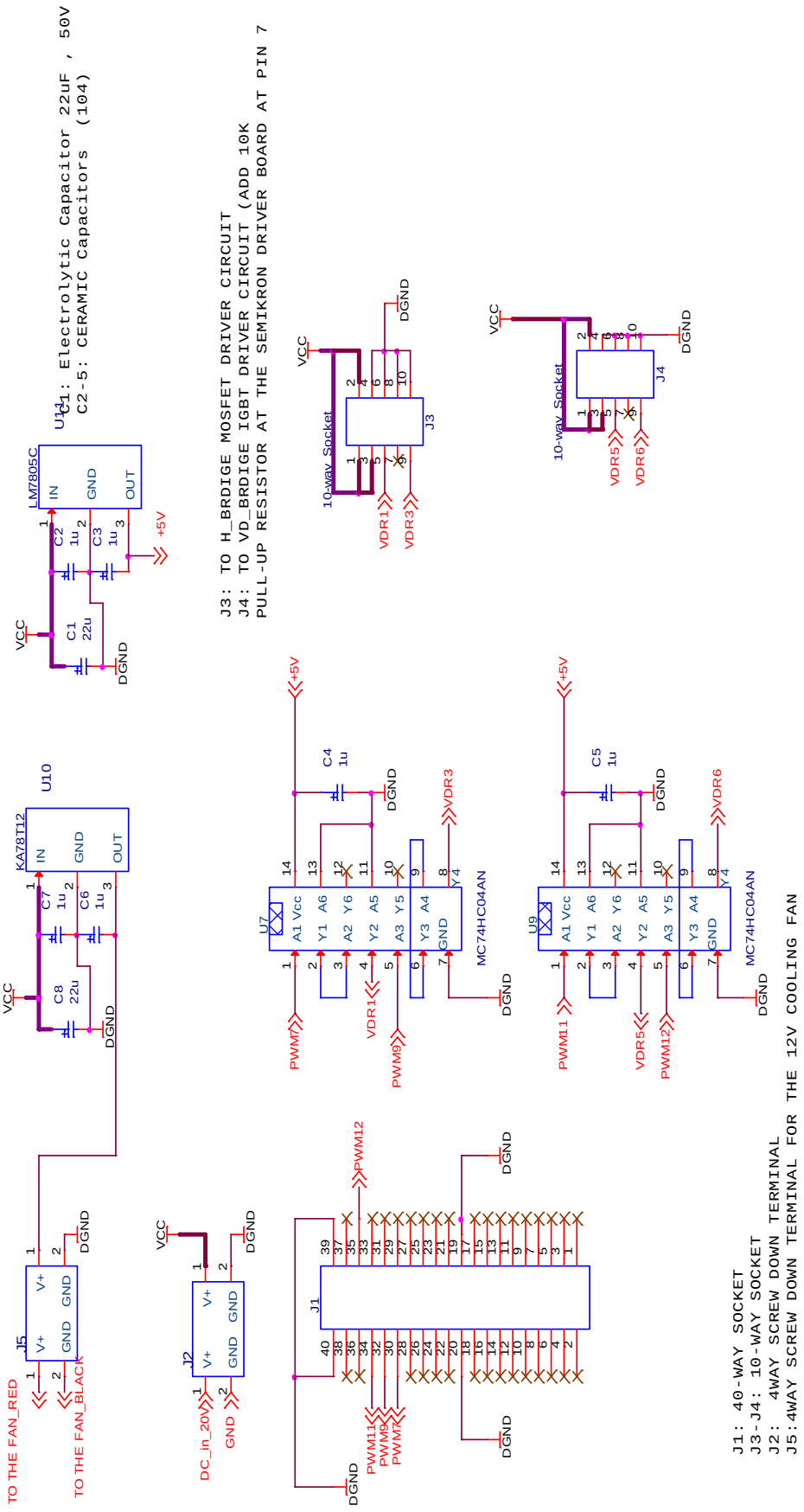


Fig. L.3 DSP-PWM interfacing circuit

Appendix M

Control Algorithm of the Proposed Optimal Modulation Scheme

```
function [PSI,PS1,PS2,Puc_min_1,Puc_max_1,Puc_min_2,Puc_max_2] =
fcn(Puc,Vuc)

%% controller algorithm of the proposed optimal modulation scheme to
ensure min CPF interval with three modes of operation for the both
power flow directions (UCCM) and (UCDM):

%%MODE ISPM:   P_uc<P_min1 &P_min2
%%MODE ZCPFM:  P_min1&2<Puc<P_max1&2
%%MODE MCPFM: Puc>P_max1&2

n=7.4;
L=10e-6;%%L=Lt
w=2*pi*20e3;
% Puc=Vuc*Iuc;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%
%%%%%%%%%%%% BOOST Operation %%%%%%%%%%%%
%%%%%%%%%%%% 2nVuc>== Vo %%%%%%%%%%%%%%%%%%%%

Puc_min_1=(1/8)*L^(-1)*n^(-2)*pi*Vo^2*Vuc^(-1)*((-1/2)*n^(-
1)*Vo+Vuc)*w^(-1); %% Pmin for boost 2nVuc>Vo %%
Puc_max_1=(1/8)*L^(-1)*n^(-
1)*pi*Vo^2*Vuc*(Vo+2*n*Vuc)*(Vo^2+2*n*Vo*Vuc+2*n^2*Vuc^2)^(-1)*w^(-
1);%% Pmax for boost 2nVuc>Vo %%
Puc_min_2=(1/8)*L^(-1)*n^(-1)*pi*Vo^(-1)*Vuc*(Vo^2+(-
4)*n^2*Vuc^2)*w^(-1);%% Pmin for boost 2nVuc<Vo %%
Puc_max_2=(1/8)*L^(-1)*n^(-
1)*pi*Vo^2*Vuc*(Vo+2*n*Vuc)*(Vo^2+2*n*Vo*Vuc+2*n^2*Vuc^2)^(-1)*w^(-
1);%% Pmax for boost 2nVuc<Vo %%


if (2*n*Vuc>=Vo)
    if(Puc>=0 && Puc < Puc_min_1)%this mode only for the small power
operation in order to get lower PSI than CPC
    PS1=0;
    PS2=((1/2).*Vo.^(-1).*Vuc.^(-
1).*(pi.*Vo.*Vuc+pi.^(1/2).*(pi.*Vo.^2.*Vuc.^2+(-
16).*L.*n.*Puc.*Vo.*Vuc.*w).^(1/2)))*(180/pi); %% inner phase-shift
angle

    elseif (Puc>=Puc_min_1 && Puc<=Puc_max_1)% this ensure PSI=0 for
particular power range limited by Puc_min and Puc_max

    Phi1= (1/2).*Vo.^(-1).*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*Vuc.^2).^(-
1).*(pi.*Vo.^3+(-
1).*(2.*pi).^(1/2).*(n.^2.*Vo.*Vuc.*(pi.*Vo.^2.*Vuc.*(Vo+2.*n.*Vuc)+(-
8).*(Puc/Vuc).*L.*n.*Vuc.*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*Vuc.^2).*w)).^
(1/2));
```

```
    PS2=(180/pi)*((1/2).*n.^(-1).*(pi+(-2).*Phi1).*Vo.*Vuc.^(-1));%
for +ve
    PS1=(180/pi)*Phi1;

    elseif (Puc>Puc_max_1)  %this ensure lower Ip and PSI
    PS2=real((((1/2)*Vo^(-1)*Vuc^(-1))*(2*pi*Vo*Vuc-
sqrt(complex(2*pi^2*Vo^2*Vuc^2+(-
16)*L*n*pi*Puc*Vo*Vuc*w))))*(180/pi));
    PS1=PS2-(90);

%%%%%%%%%%%% Buck Operation %%%%%%%%%%%%
%%%%%%%%%%%% 2nVuc>== Vo %%%%%%%%%%%%%%%%%%%%

    elseif (Puc<0 && Puc > -Puc_min_1)
    PS1=0;
    PS2=((1/2).*Vo.^(-1).*Vuc.^(-1).*((-1).*pi.*Vo.*Vuc+(-
1).*pi.^(1/2).*(
pi.*Vo.^2.*Vuc.^2+16.*(Puc/Vuc).*L.*n.*Vo.*Vuc.^2.*w).^(1/2)))*(180/pi
);

    elseif (Puc<= -Puc_min_1 && Puc>= -Puc_max_1)% this ensure PSI=0
    Phi1=(1/8).*Vo.^(-1).*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*Vuc.^2).^(-
1).*(( -
4).*pi.*Vo.^3+4.*(2.*pi).^(1/2).*(n.^2.*Vo.*Vuc.*(pi.*Vo.^2.*Vuc.*(Vo+
2.*n.*Vuc)+8.*L.*n.*Puc.*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*
Vuc.^2).*w)).^(1/2));
    PS2=(180/pi)*((-1/2).*n.^(-1).*(pi+2.*(Phi1)).*Vo.*Vuc.^(-1));
    PS1=(180/pi)*Phi1;


    else %this ensure lower Ip and PSI
     PS2=real((((1/2).*Vo.^(-1).*Vuc.^(-1))*((-
2).*pi.*Vo.*Vuc+sqrt(complex(2.*pi.*(pi.*Vo.^2.*Vuc.^2+8.*L.*n.*Puc.*V
o.*Vuc.*w)))))*(180/pi));
     PS1=PS2+(90);
    end
    %%the following equations are to determine PSI value for different
mode
    %%for the boost and buck operation under 2nVuc>Vo condition
        if(PS1>=0 && PS2>=0)
        PSI=(180/pi)*((1/2).*((1/2).*Vo+n.*Vuc).^(-1).*((-
1/2).*pi.*Vo+(PS1*(pi/180)).*Vo+n.*(PS2*(pi/180)).*Vuc)); %% for boost
        else
        PSI=(180/pi)*((1/2).*((1/2).*Vo+n.*Vuc).^(-
1).*((1/2).*pi.*Vo+(PS1*(pi/180)).*Vo+n.*(PS2*(pi/180)).*Vuc)); %% for
Buck
        end

%%%%%%%%%%%% BOOST Operation %%%%%%%%%%%%
%%%%%%%%%%%% 2nVuc<= Vo %%%%%%%%%%%%%%%%%%%%

else

    if(Puc>=0 && Puc < Puc_min_2)
    PS1=0;
    PS2=((1/2).*Vo.^(-1).*Vuc.^(-
1).*(pi.*Vo.*Vuc+pi.^(1/2).*(pi.*Vo.^2.*Vuc.^2+(-
16).*L.*n.*Puc.*Vo.*Vuc.*w).^(1/2)))*(180/pi);

    elseif (Puc>=Puc_min_2 && Puc<=Puc_max_2)
```

```
    Phi1= (1/2).*Vo.^(-1).*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*Vuc.^2).^(-
1).*(pi.*Vo.^3+(-
1).*(2.*pi).^(1/2).*(n.^2.*Vo.*Vuc.*(pi.*Vo.^2.*Vuc.*(Vo+2.*n.*Vuc)+(-
8).*(Puc/Vuc).*L.*n.*Vuc.*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*Vuc.^2).*w)).^
(1/2));
    PS2=(180/pi)*((1/2).*n.^(-1).*(pi+(-2).*Phi1).*Vo.*Vuc.^(-1));%
for +ve%
    PS1=(180/pi)*Phi1;

    elseif (Puc>Puc_max_2)
    PS2=real((((1/2)*Vo^(-1)*Vuc^(-1))*(2*pi*Vo*Vuc-
sqrt(complex(2*pi*(pi*Vo^2*Vuc^2+(-8)*L*n*Puc*Vo*Vuc*w)))))*(180/pi));
    PS1=PS2-(90);

%%%%%%%%%%%% Buck Operation %%%%%%%%%%%%%
%%%%%%%%%%%% 2nVuc<= Vo %%%%%%%%%%%%%%%%%%%%

    elseif(Puc<0 && Puc > -Puc_min_2)
    PS1=0;
    PS2=((1/2).*Vo.^(-1).*Vuc.^(-1).*((-1).*pi.*Vo.*Vuc+(-
1).*pi.^(1/2).*(pi.*Vo.^2.*Vuc.^2+16.*L.*n.*Puc.*Vo.*Vuc.*w).^(1/2)))*
(180/pi);

    elseif (Puc<= -Puc_min_2 && Puc>= -Puc_max_2)
    Phi1=(1/8).*Vo.^(-1).*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*Vuc.^2).^(-
1).*(( -
4).*pi.*Vo.^3+4.*(2.*pi).^(1/2).*(n.^2.*Vo.*Vuc.*(pi.*Vo.^2.*Vuc.*(Vo+
2.*n.*Vuc)+8.*L.*n.*Puc.*(Vo.^2+2.*n.*Vo.*Vuc+2.*n.^2.*
Vuc.^2).*w)).^(1/2));
    PS2=(180/pi)*((-1/2).*n.^(-1).*(pi+2.*(Phi1)).*Vo.*Vuc.^(-1));
    PS1=(180/pi)*Phi1;

    else
     PS2=real((((1/2).*Vo.^(-1).*Vuc.^(-1))*((-
2).*pi.*Vo.*Vuc+sqrt(complex(2.*pi.*(pi.*Vo.^2.*Vuc.^2+8.*L.*n.*Puc.*V
o.*Vuc.*w)))))*(180/pi));
     PS1=PS2+(90);

    end
%%the following equations are to determine PSI value for different
mode
%%for the boost and buck operation under 2nVuc<Vo condition
       if(PS1>=0 && PS2>=0)
        PSI=(180/pi)*((1/2).*((1/2).*Vo+n.*Vuc).^(-1).*((-
1/2).*pi.*Vo+(PS1*(pi/180)).*Vo+n.*(PS2*(pi/180)).*Vuc)); %% for boost
        else
        PSI=(180/pi)*((1/2).*((1/2).*Vo+n.*Vuc).^(-
1).*((1/2).*pi.*Vo+(PS1*(pi/180)).*Vo+n.*(PS2*(pi/180)).*Vuc)); %% for
Buck
        end

end
```

Glossary and Terms

List of Symbols

SYMBOL	UNIT	DESCRIPTION
C_o	F	Output filter capacitance of the full bridge rectifier
C_1 and C_2	F	Output filter capacitances of the voltage-doubler circuit
C_a	F	Clamp capacitance
C_p	F	Parasitic capacitance of the switch devices
C_{dl}	F	Equivalent capacitance of double-layer effect
C	F	Voltage–independent capacitance
C_{co}	F	Constant capacitance
C_{uc}	F	Capacitance of each cell of the ultracapacitor
C_i	F	Capacitance utilised to cancel the effect of R_i at high frequencies
C_v	F	Non-linear capacitance
C_{int}	F	Inter-winding capacitance of the transformer
d(t)	—	Dynamic duty cycle including the conduction of anti-parallel diodes
d'(t)	—	Complementary duty cycle including the discharge period of parasitic capacitances
D	—	Steady-state duty cycle
D'	—	Complementary steady-state duty cycle
D_{eff}		Effective overlap duty cycle
δ	—	Fraction of the period during which energy is transferred from the leakage inductance to the secondary side
Δ	—	Steady-state value of δ
ΔV_{ohmic}, ΔV_{conc}, and ΔV_{activ}	V	Voltage drop due to the concentration, ohmic, and activation losses respectively
ΔP_{load}	W	Transient power
E_{uc}	Wh	Available Energy stored in the ultracapacitor
E_{SW_off}	Joul	Energy dissipate in clamp switch during device turn-off
E_{Ca}	Joul	Circulating energy caused by active-clamp circuit
f_{r1} and f_{r2}	Hz	Resonant frequency due to interaction of parasitic elements
f_c	Hz	Cross-over frequency
f_s	Hz	Switching frequency
φ	Degree	Phase-shift between two bidirectional converter bridges using CPC modulation
φ_1	Degree	Phase-shift between two bidirectional converter bridges using proposed modulation
φ_2	Degree	Inner phase-shift
φ_{max}^{CPC}	Degree	Maximum phase-shift by CPC modulation
φ_{max}^{TRM}	Degree	Maximum phase-shift by TRM method
φ_{max}^{PTRM}	Degree	Maximum phase-shift by PTRM method
$\varphi_{1\_ZCPF}^{min,b}$	Degree	Minimum inner phase-shift by ZCPF modulation for $2nV_{uc} > V_o$ and UCDM
$\varphi_{2_{ZCPF}}^{min,b}$	Degree	Minimum phase-shift by ZCPF modulation for $2nV_{uc} > V_o$ and UCDM
$\varphi_{1\_ZCPF}^{min,c}$	Degree	Minimum inner phase-shift by ZCPF modulation for $2nV_{uc} < V_o$ and UCDM
$\varphi_{2_{ZCPF}}^{min,c}$	Degree	Minimum phase-shift by ZCPF modulation for $2nV_{uc} < V_o$ and UCDM
$\varphi_{1\_ZCPF}^{max,b}$	Degree	Maximum inner phase-shift by ZCPF modulation for $2nV_{uc} > V_o$ and UCDM
$\varphi_{2\_ZCPF}^{max,b}$	Degree	Maximum phase-shift by ZCPF modulation for $2nV_{uc} > V_o$ and UCDM
$\varphi_{1\_ZCPF}^{min,d}$	Degree	Minimum inner phase-shift by ZCPF modulation for $2nV_{uc} > V_o$ and UCCM

$\varphi_{2_{ZCPF}}^{min,d}$	Degree	Minimum phase-shift by ZCPF modulation for $2nV_{uc} > V_o$ and UCCM
$\varphi_{1\_ZCPF}^{min,e}$	Degree	Minimum inner phase-shift by ZCPF modulation for $2nV_{uc} < V_o$ and UCCM
$\varphi_{2_{ZCPF}}^{min,e}$	Degree	Minimum phase-shift by ZCPF modulation for $2nV_{uc} < V_o$ and UCCM
$\varphi_{1\_ZCPF}^{max,d}$	Degree	Maximum inner phase-shift by ZCPF modulation for $2nV_{uc} > V_o$ and UCCM
$\varphi_{2\_ZCPF}^{max,d}$	Degree	Maximum phase-shift by ZCPF modulation for $2nV_{uc} > V_o$ and UCCM
GPxT	——	General purpose timer
K_{pv} K_{iv} K_{pc} K_{ic}	——	Constant values of the analogue PI controllers for the current and voltage loop
K_{ov} K_{qv} K_{oc} K_{qc}	——	Constant values of the digital PI controllers for the current and voltage loop
K_v	——	Non–linear function of the ultracapacitor voltage
L_D+L_S	H	Switch stray inductances
L_b	H	Boost inductance
L_σ	H	Leakage inductance referred to the primary side of the transformer
L_t	H	Series inductance
L_{ext}	H	External inductance
$L_{\sigma 2}$	H	Leakage inductance of the secondary windings
$i_{C1}(t)$	A	Current in C_1
$i_{C2}(t)$	A	Current in C_2
$i_{Ca}(t)$	A	Current in C_a
$i_{L\sigma}(t)$	A	Primary current
$i_{Lb}(t)$	A	Input/boost inductor current in L_b
$\overline{I_{Lb}}$	A	Steady-state average input current in L_b
$I_{L\sigma}$	A	Steady-state average primary current
$i_{Lt}(\theta)$	A	Instantaneous primary current via BDC transformer
I_{to}, I_ϕ, I_π, $I_{\pi+\varphi}$ I_{to} $I_{\varphi 1}$ $I_{\varphi 2}$ I_π, $I_{\pi+\varphi 1}$ $I_{\pi+\varphi 2}$	A	Values of currents at the commutation instants
I_{rms}	A	RMS current through the transformer
I_p	A	Peak current in L_σ
M	——	Voltage conversion ratio of the converter
n	——	Transformer turn ratio
N_{uc}	——	Number of cell
ω	rad/s	Angular frequency
P_{uc}	W	Average power of ultracapacitor
P_{load}	W	Average load power
P_{fc}	W	Average fuel cell power
P_{uc}^{max}	W	Maximum achievable power for CPC
P_{uc}^{PTRM}	W	Maximum achievable power for PTRM method
$P_{uc\_max}^{TRM}$	W	Maximum achievable power for TRM method
$P_{uc\_ISP}^{max}$	W	Maximum achievable power for ISP scheme
$P_{uc\_ZCPF}^{min,b}$	W	Minimum achievable power by ZCPF modulation for $2nV_{uc} > V_o$ and UCDM
$P_{uc\_ZCPF}^{min,c}$	W	Minimum achievable power by ZCPF modulation for $2nV_{uc} < V_o$ and UCDM
$P_{uc\_ZCPF}^{mind}$	W	Minimum achievable power by ZCPF modulation for $2nV_{uc} > V_o$ and UCCM
$P_{uc\_ZCPF}^{min,e}$	W	Minimum achievable power by ZCPF modulation for $2nV_{uc} < V_o$ and UCCM
$P_{uc\_ZCPF}^{max,b}$	W	Maximum achievable power by ZCPF modulation for UCDM
$P_{uc\_ZCPF}^{max,d}$	W	Maximum achievable power by ZCPF modulation for UCCM
$P_{uc\_ZCPF\_L}^{b}$	W	Achievable power by ZCPF for low power operation for $2nV_{uc} > V_o$ and UCDM
$P_{uc\_ZCPF\_L}^{c}$	W	Achievable power by ZCPF for low power operation for $2nV_{uc} < V_o$ and UCDM
$P_{uc_{ZCPF_H}}^{b}$	W	Achievable power by ZCPF for high power operation for $2nV_{uc} > V_o$ and UCDM

PWM1 to PWM12	——	Pulse-width modulation of generated by the DSP
PS1and PS2	Degree	Phase-shift used for Simulink results
ψ	Degree	Circulating power flow interval
Q_{rev}	C	Reverse-recovery charge
R_{fc}	Ω	Fuel cell internal resistance
R_{act}	Ω	Activation resistance
R_{con}	Ω	Concentration resistance
R_p	Ω	self-discharge resistance
R_{esr}	Ω	Equivalent series resistance
R_v	Ω	ESR DC resistance
R_i	Ω	Ionic resistance in the electrolyte
S_1~S_2, S_3~S_4,	——	MOSFETs
Z_1~Z_2	——	IGBTs
T_s	sec	Switching time period
T_E	sec	Overlap time period
$T_i(s)$	——	Open-loop transfer function of current loop
$T_v(s)$	——	Open-loop transfer function of voltage loop
T_d	sec	Computational delay time
T_{sa}	sec	Sampling time
T1		Timer 1
T2		Timer 2
T_1…..T_n		Mode intervals
$v_{ca}(t)$	V	Instantaneous clamp capacitor voltage
$v_{C1}(t)$ and $v_{C2}(t)$	V	Instantaneous output capacitor voltages
V_{C1} and V_{C1}	V	Average voltage-doubler capacitor voltages
$V_{uc\ min}$	V	Minimum ultracapacitor voltage can be utilised by the BDC
$V_{uc\ max}$	V	Maximum ultracapacitor voltage
$v_o(t)$	V	Instantaneous output voltage
$v_{Lb}(t)$	V	Instantaneous boost inductor voltage
V_o	V	Average output voltage
V_{Ca}	V	Average clamp capacitor voltage
V_{uc}	V	Rated ultracapacitor Voltage
V_{fc}	V	fuel cell Voltage
V_{fc_o}		Open circuit fuel cell Voltage
V_{LB}	V	Average boost inductor voltage
$v_{pri(t)}$	V	Primary voltage
$v'_{sec(t)}$	V	Instantaneous secondary voltage referred to the primary
$v_{Lt(t)}$	V	Instantaneous series inductance voltage
$\langle v_{ca}(t)\rangle_{T_s}$ $\langle v_{\sigma}(t)\rangle_{T_s}$ $\langle v_o(t)\rangle_{T_s}$ $\langle v_{Lb}(t)\rangle_{T_s}$ $\langle v_{fc}(t)\rangle_{T_s}$	V	Low-frequency averaged values
$\hat{v}_{Lb}(t), \hat{v}_{fc}(t)$ $\hat{v}_{\sigma}(t), \hat{v}_o(t)$ $\hat{\delta}(t), \hat{d}(t)$ $, \hat{i}_{Lb}(t)$ $\hat{i}_{\sigma}(t), \hat{i}_c(t)$	V	Small ac variation components
V_v	V	Voltage across C_v
$v_{Ca\ max}(t)$	V	Maximum voltage across C_a

Abbreviations

NAME	DESCRIPTION
APM	Alternative phase-shift modulation
BDC	Bidirectional DC–DC converter
CPC	Conventional phase-shift control
CHP	Combined heat and power
CFC	Current-fed converter
CMPR	Compare register
DSP	Digital signal processing
FBCFC	Full bridge current-fed converter
FC	Fuel cell
HSW	Hard-switching
ISPM	Inner single phase-shift mode
MCPFM	Minimum circulating power flow mode
MTRM	Modified triangular current modulation
PV	Photovoltaic
PTRM	Proposed triangular current modulation
PEMFC	Proton exchange membrane fuel cell
RHPZ	Right–half–plane–zero
RTDX	Real Time Data Exchange feature
SOC	State-of-charge
SSW	Soft-switching
TRM	Triangular current modulation
TZM	Trapezoidal current modulation
TRI	Triangular carrier signal
UC	Ultracapacitor
UCCM	Ultracapacitor charging mode
UCDM	Ultracapacitor discharging mode
VFC	Voltage-fed converter
WECS	wind energy conversion system
ZVS	Zero-voltage switching
ZCS	Zero-current switching
ZCPFM	Zero circulating power flow mode

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