Investigation on Degradation of SiC MOSFET under Surge Current Stress of Body Diode

Xi Jiang[1], Jianjun Chen[1], Jun Wang[1], *Senior Member, IEEE*, Zongjian Li[1], Dongyuan Zhai[1], Xin Yang[1], Bing Ji[2], *Member, IEEE*, Z. John Shen[3], *Fellow*, *IEEE*
[1]College of Electrical and Information Engineering, Hunan University, Changsha, China
[2]Department of Engineering, University of Leicester, Leicester, UK
[3]Illinois Institute of Technology, Chicago, IL, USA
Email: junwang@hnu.edu.cn

Abstract- **Eliminating antiparallel SiC SBD and making use of the intrinsic body diode of SiC MOSFET offers a cost-effectiveness solution without obviously sacrificing the conversion efficiency in some power converter applications. Although the body diode of commercial SiC MOSFET has been qualified by several manufacturers, the reliability of SiC MOSFET under repetitive surge current stress of body diode has not been sufficiently studied. In this paper, the new degradation phenomena of SiC MOSFET's gate oxide is observed, and the degradation mechanism is discussed when the intrinsic body diode of 1200V SiC planar gate MOSFETs was subjected to surge current stress. TCAD simulation and experimental measurements indicate that the generation and accumulation of electrons or holes within the gate oxide under surge current stress are root reasons for the degradation of SiC MOSFET. Finally, a mitigation technique with optimal gate turn-off voltage is suggested to suppress the gate oxide degradation of the SiC MOSFET under the surge current stress of its body diode.**

***Index Terms*—SiC MOSFET, surge current, body diode, gate oxide degradation, gate control**

I. INTRODUCTION

Silicon carbide metal-oxide-semiconductor-field-effect transistors (SiC MOSFETs) outperform silicon (Si) insulated gate bipolar transistors (IGBTs) in terms of high efficiency and high power density in power converter applications because of their superior performance including low conduction loss, fast switching speed and high switching frequency capability [1], [2]. Usually, SiC Schottky barrier diode (SBD) was anti-paralleled to the SiC MOSFETs as a freewheeling diode in the power converter applications because it has a relatively low forward voltage drop and no reverse recovery current. However, SiC SBD is approximately four times more expensive than Si FRD [3]. This solution inevitably causes unfavorable consequences, such as higher die cost and larger assembling area in the power module. Meanwhile, the external SiC SBD only conducts during the dead time and results in a minor increase in conversion efficiency at traditional switching speed power converters [4]. Therefore, the implementation of extra SiC SBD as an anti-parallel diode to SiC MOSFET is not a favorable solution in many cost-sensitive power conversion application cases because of its high cost.

Removing the antiparallel SiC SBDs from SiC MOSFET/SiC SBD pair is a favorable and cost-effective solution for these applications without obviously sacrificing power conversion efficiency. In recent years, many studies on the feasibility and benefits of utilizing the body diode of SiC MOSFETs in power applications without anti-paralleled SiC SBD have been reported. Although the effect of the body diode of SiC MOSFET on conversion efficiency is influenced by temperature and switching frequency, removing antiparallel SBDs is recommended for traditional switching speed applications [5],[6]. Synchronous rectification operation of SiC MOSFET without anti-paralleled SiC SBD can achieve almost the same conversion efficiency of the inverter as a conventional inverter using SiC SBD as freewheeling diode [4],[5]. It is mainly because the synchronous rectification operation of SiC MOSFET can significantly reduce the reverse conduction losses, and MOSFET's body diode only conducts current during a very short dead time. Moreover, it has been reported that removing additional SBDs exhibits large advantage in terms of power loss and EMI characteristics in inverter applications especially for smaller current or lower temperature operation conditions [5],[7]. This enables system designers to squeeze out the current capability and to capitalize on the benefits of SiC MOSFETs. At the same time, continuous improvements in the performance of body diode of the SiC MOSFETs have been made by manufacturers of SiC devices [8]. Recently, SiC MOSFET's body diode has demonstrated excellent reverse recovery characteristics, which is comparable to the SiC SBD [6].

Concerns on reliability and surge current ruggedness of 1200-1700V commercial SiC MOSFET's body diode needs to be addressed for its converter applications requiring reverse conduction. First, there are stability and bipolar degradation concerns on SiC MOSFETs' intrinsic body diodes in the early stage of SiC MOSFETs' commercialization. When forward current is applied to the PN body diode of SiC MOSFETs, a crystal defect called stacking faults may expand from pre-existing basal plane dislocations (BPDs) due to the recombination energy of electrons and holes [9]. The stacking faults inside the SiC device act as a resistance, which increases the forward voltage drop of the body diode [10]. Due to the rapid development of SiC material epitaxy technology and improved manufacture process control, the body diode of the latest 2-3 generation SiC MOSFETs has been qualified by several manufacturers and exhibited excellent stability. The body diode of SiC MOSFET shows stable performance under 1000 hours of accelerated stressing tests [11]. Long-term switching converter testing shows the reliable operation of SiC MOSFET's body diode for over 10,000 hours, and no bipolar degradation was observed [12]. Second, excellent surge current capability of the body diode of SiC MOSFET is required to be capable of withstanding several folds of the rated current for a short time interval during the start-up process of a power factor correction (PFC) or certain fault conditions in a voltage source inverters of the motor-driven load [13]. Characterization study of the surge current capability of SiC MOSFET's body diodes and failure mechanism analysis under singe surge current pulse condition are presented in [14]-[16]. Comparative evaluations among Si-PiN diode, SiC Junction Barrier Schottky (JBS) diode, and SiC MOSFET's body diodes have been reported [16],[17], the

experimental results show that the SiC MOSFET's body diodes have a slightly better surge current capability than the same current rating SiC JBS diode. A short circuit of the gate-source terminals of SiC MOSFET was observed under surge current stress of body diode [14]. Thermal model simulation and microscopy failure analysis reveal that the junction temperature increase above the melting point of the surface aluminum metallization is the reason for the gate failure [18],[19].

Although the excellent surge current ruggedness and stability of commercial SiC MOSFET's body diode under normal operation conditions and single surge current pulse stress have been demonstrated, there has been no report on the influence of repetitive surge current stress of SiC MOSFET's intrinsic body diode on the reliability of SiC MOSFET. Reliability study of 10-kV SiC MOSFET research sample has shown forward stress on body diode can induce the increase of on-resistance and drain leakage current of SiC MOSFET [9]. Investigation and analysis are needed to make sure whether repetitive surge current stress of body diode induces reliability issue of commercial SiC MOSFET. If it is true, the degradation mechanism and the suppression method are expected for the adoption of SiC MOSFET's body diode in the commercial power conversion applications.

The purpose of this paper is to demonstrate the degradation phenomena of commercial SiC MOSFET under repetitive surge current stress of its intrinsic body diode, study the degradation mechanism and propose a mitigation technique to suppress the device degradation. The organization of the paper is as follows. Section II presents the surge current test and degradation phenomena of 1200V commercial SiC MOSFET under repetitive surge current stress of its intrinsic body diode. The influence of major limiting factors, including surge current magnitude, negative gate turn-off voltage, surge current cycle numbers are experimentally studied. In Section III, the electro-thermal TCAD simulation was carried out to investigate the gate oxide degradation mechanism of the SiC MOSFET under surge current of the body diode. Meanwhile, the degradation mechanism is verified by the subthreshold voltage measurement, capacitance-voltage characteristics and high temperature recovery treatment after the surge current stress. In Section IV, a mitigation technique with gate voltage optimization is proposed to suppress the performance degradation of the SiC MOSFET. Finally, Section V concludes this paper.

II. Surge Current Stress and Degradation Phenomena

A. *Test Setup*

A simplified schematic of the surge current capability test circuit and the test platform are shown in Fig.1 and Fig.2, respectively. The adjustable AC voltage source outputs 50 Hz sinusoidal voltage. Two IGBTs (IXYS IXGK120N120A3) [20] with high current rating are parallel-connected to increase the current handling capability. They are serially connected with the device under test (DUT) to control the duration of the current surge pulse applied to the DUT. The test procedures comply with the JEDEC Standard No. 282B.01 [21], where the DUT is stressed under up to 100 surge current pulses with a duration of 10 ms

each. The interval time between each surge current pulse is set to be 20 s. A heat sink with fan cooling was used to allow the DUT to return to thermal equilibrium at room temperature after each surge current pulse to counteract the influence of thermal accumulation. After applying a trigger signal, the DSP detects the positive half-sinusoidal wave from a Hall effect voltage sensor, and the IGBT Q_1 is turned on at the zero-crossing point of the full-wave rectifier. The amplitude of the surge current can be changed by adjusting the input voltage. The surge current tests were carried out at room temperature (25°C).

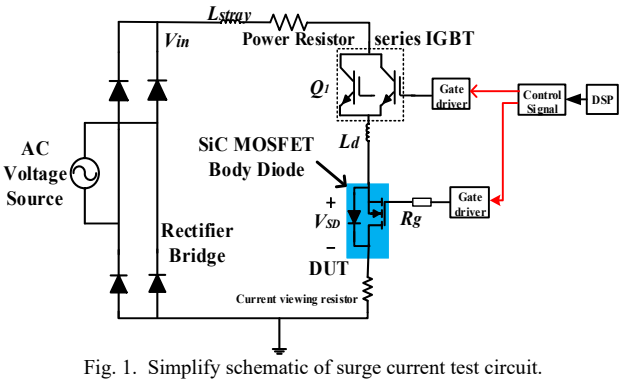


Fig. 1. Simplify schematic of surge current test circuit.

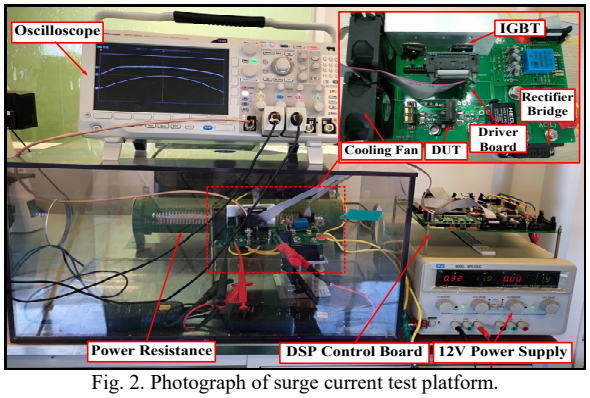


Fig. 2. Photograph of surge current test platform.

In this study, the non-repetitive peak surge current (I_{FSM}) of the SiC MOSFET's body diode is determined whenever any of the following cases happen. The DUT is failed, or its electrical parameters are out of the specification defined by its datasheet after surge current stress. The experiments are conducted with the commercial SiC planar gate MOSFETs rated at 1200 V/12.5 A in a TO-247 package [22]. Three samples are used for each test under the same stress conditions to confirm the variation of the electrical parameters.

B. Characterization and Surge Current Capability

In this part, the forward conduction characteristics and surge current capability of the SiC MOSFET's body diode under different gate turn-off voltages are analyzed. Three different levels of gate turn-off voltage (V_{gs_off}) were compared along with the surge current conditions. The V_{gs_off} was set to be 0V, -5V and -10V, respectively. The forward conduction characteristics of the body diode of the SiC MOSFET at different V_{gs_off} are shown in Fig. 3, which is plotted on the V_{ds}-I_d coordinates of the MOSFET. The forward voltage drop of SiC MOSFET's body diode at zero gate turn-off voltage is smaller than that at negative gate turn-off voltage condition. This is because a positive potential appearing at the p-body to n-SiC interface and an inversion MOS channel is formed [23], resulting in partial current flowing through the MOSFET channel. When the gate voltage decreases to a relatively large negative value, the inversion MOS channel is closed, and essentially the forward conduction characteristics of the body diode manifest. The forward voltage drop of the body diode almost keep the same when the gate turn-off voltage is negatively increased from -5V to -10 V.

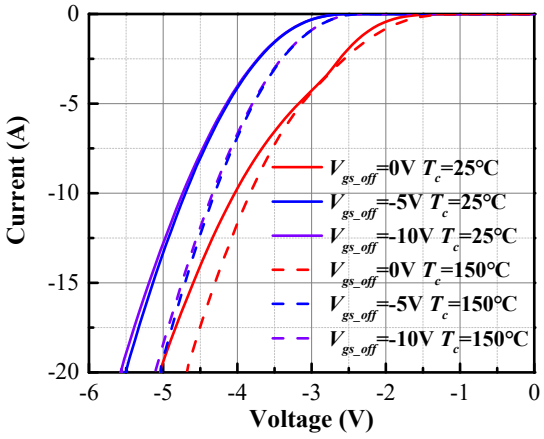


Fig. 3 Forward conduction characteristics of SiC MOSFET's body diode at different V_{gs_off}.

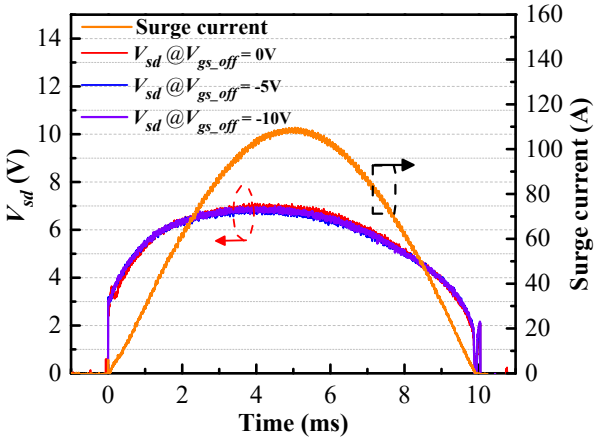


Fig. 4 Measured surge current and forward voltage drop waveforms of body diode at different V_{gs_off}. (The surge current capability is independent of the V_{gs_off})

The non-repetitive surge current with a peak surge current of 110A in association with the forward voltage drop of the body diode is depicted in Fig. 4, along with the gate turn-off voltage conditions. A sinusoidal surge current was applied to the device for a duration of 10 ms. Due to the wide bandgap of the silicon carbide material, the body diode of the SiC MOSFET exhibits a large forward voltage drop as compared with its silicon counterpart, which is around 2.8V when the forward current is small at around 0 ms. High surge current flowing through the body diode of SiC MOSFET induces large power loss. Thus, junction temperature increases rapidly due to the self-heating of the device. However, the injection of minority carriers by the PN junctions clamps the increasing forward voltage drop with the increase of the surge current, which suppresses the power surge and limits the further increase of the junction temperature. The forward voltage drop of body diode increases to a maximum of approximately 6.9 V at 5ms. Although the forward voltage drop of the body diode decreases with the increase of gate turn-off voltage at nominal current, the peak forward voltage drop under surge current is almost the same when the V_{gs_off} is varying from the -10 V to 0 V. This can be explained by that all the current flow through the PN junction under surge current conditions. Therefore, the surge current capability of the SiC MOSFET's body diode is independent of the gate turn-off voltage.

All the tested SiC MOSFETs are failed after a peak surge current stress of 120 A. Inspection of the failed devices shows that the SiC MOSFET's gate-source terminals are shorted while its drain-source PN junction retains the blocking capability. But the breakdown voltage of the degraded device has been reduced to 800 V. Thereby, the I_{FSM} of the body diode of the 1200 V/12.5 A SiC MOSFET is defined to 110 A according to the criteria as mentioned above.

In order to investigate the limiting factor for device degradation under surge current stress, the devices was tested under various surge current magnitude and gate turn-off voltage levels. The SiC MOSFET's electrical parameters are characterized by a

Keysight B1505A curve tracer, including the forward voltage drop of body diode (V_{sd}), drain-source leakage current (I_{dss}), threshold voltage (V_{th}) and on-state resistance ($R_{ds(on)}$) characteristic. The changes in electrical parameters are periodically measured before stress and after each set of surge current test. All the static characteristic measurements are performed at room temperature.

C. Influence of Surge Current Magnitude on Performance Degradation

The test started with an initial peak surge current of 50A, and the amplitude of the current was increased step by step until reach to I_{FSM}. The DUTs were subjected to 100 cycles surge current pulses at each current level. Fig. 5 shows the variation of the V_{sd} and I_{dss} with the increase of surge current under -5V gate turn off voltage, respectively. In order to prevent the effects of inversion MOS channel on the forward voltage drop of the body diode caused by gate oxide degradation, the V_{sd} was measured at a gate voltage of -10 V and drain current (I_{sd}) of 10 A. The results show that there is only a minor increase in the V_{sd} of the SiC MOSFET. After a peak surge current of 110 A, the V_{sd} of the body diode increased by 1.3 % from its initial value. At the same time, the I_{dss} increased by 51 % after a peak surge current of 110 A.

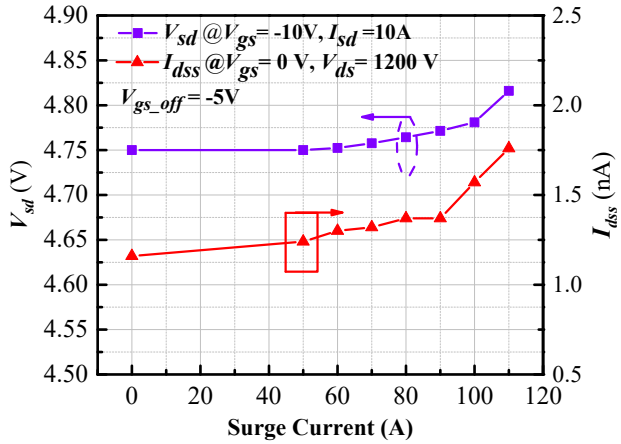


Fig. 5. Evolution of V_{sd} and I_{dss} with the increase of surge current under V_{gs_off} = -5 V.

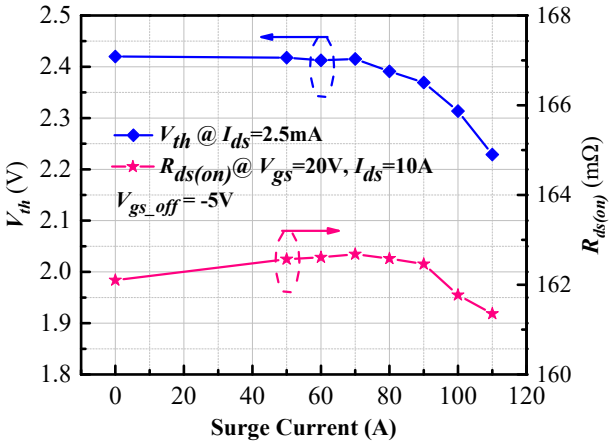


Fig. 6. Evolution of V_{th} and $R_{ds(on)}$ with the increase of surge current under V_{gs_off} = -5V.

As the surge current stress increases, the variation of V_{th} and $R_{ds(on)}$ is more significant. Fig. 6 shows the variation of the V_{th} and $R_{ds(on)}$ with the increase of surge current under -5V gate turn-off voltage condition, respectively. The V_{th} of SiC MOSFET is defined as the gate-source voltage when the gate and drain terminals are shorted, and the drain current is equal to 2.5mA. The figure shows a gradual decrease in V_{th} with surge current stress. After the surge current test with a peak surge current of 110 A, the V_{th} of the SiC MOSFET decreased by 8 % from its initial value. It indicates that the gate oxide degradation occurs in SiC MOSFET under surge current stress. The $R_{ds(on)}$ of the stressed devices was extracted by I-V measurement at a gate voltage of 20

V and drain current (I_{ds}) of 10 A. The $R_{ds(on)}$ slightly increases first and then decreases with the surge current stress. After a peak surge current of 110 A, the $R_{ds(on)}$ decreased by 0.5 % from its initial value. This phenomenon may be caused by the competition of different mechanisms that impact the measured on-state resistance. With the increase of surge current stress, the SiC/SiO_2 interface traps density gradually increase. At the initial stage, the increasing density of interface traps that lead to strong Coulomb scattering at the interface charges and thus significantly reduce the channel mobility [24]. Therefore, the $R_{ds(on)}$ shows an increasing trend. At the later stage, holes accumulate in the oxide traps inducing an additional electric field is build up across the gate oxide. This results in an obvious reduction of threshold voltage and thereby the decrease of $R_{ds(on)}$. Furthermore, the gate leakage current of SiC MOSFETs is also measured and shows no increase of gate leakage current after each set of surge current test. It means that there is no conductive path formed in the gate oxide with the increase of surge current stress.

D. Influence of Gate Turn-off Voltage on Performance Degradation

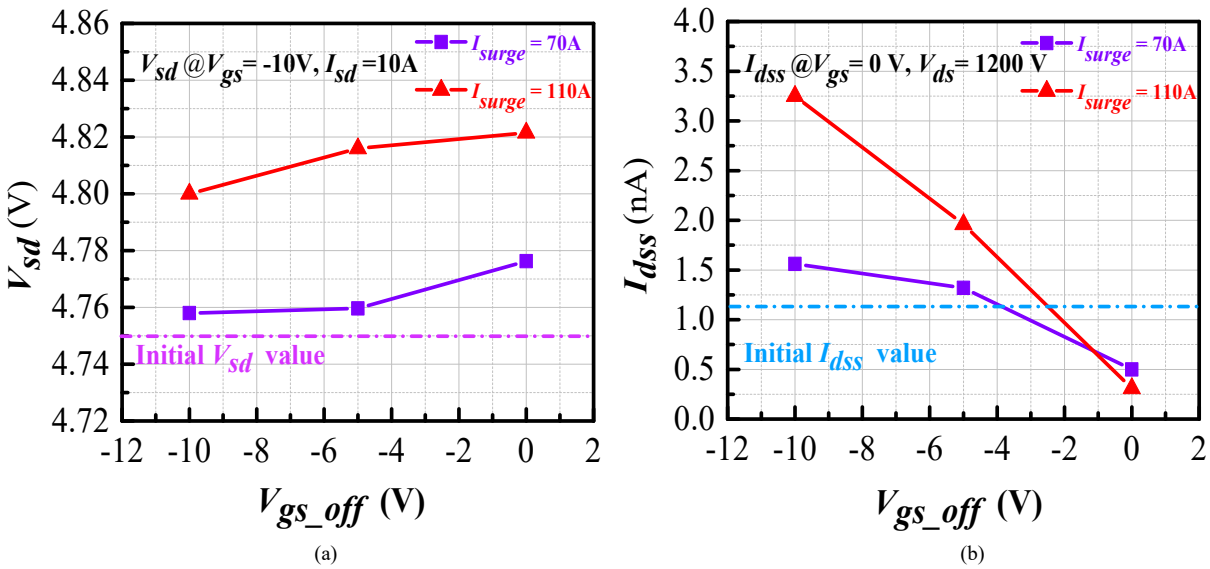
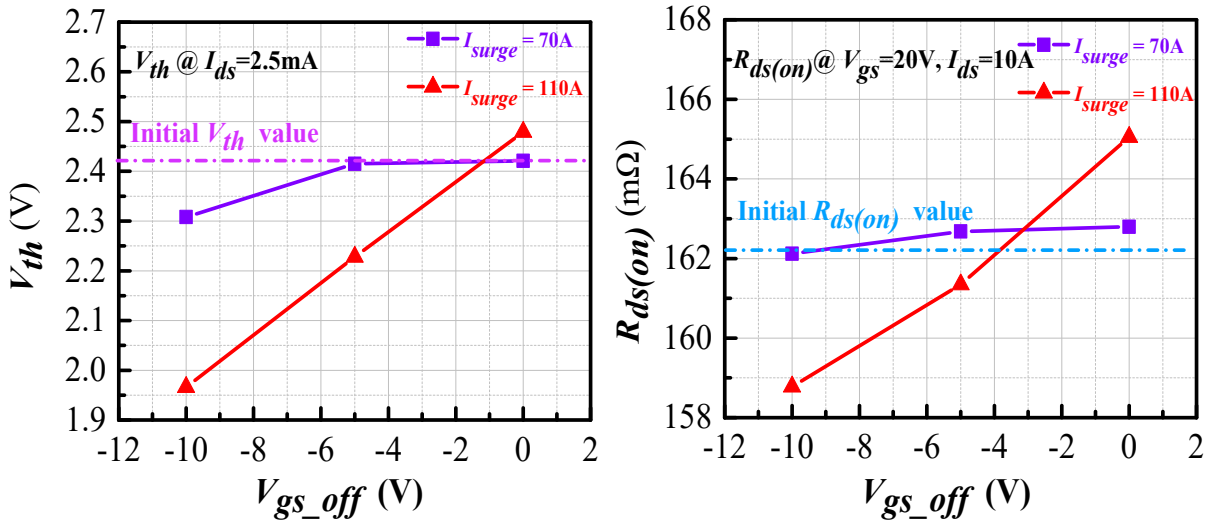


Fig. 7. (a) Evolution of V_{sd} with different gate turn-off voltage after 70A and 110A surge current stress. (b) Evolution of I_{dss} with different gate turn-off voltage after 70A and 110A surge current stress.

Three different levels of gate turn-off voltage were compared to figure out the influence of negative gate turn-off voltage on SiC MOSFET under surge current stress. The DUTs were subjected to 100 cycles surge current pulses at each gate turn-off voltage levels. Fig. 7 shows the evolution of the V_{sd} and I_{dss} at different gate turn-off voltage levels after 70A and 110A surge current stress, respectively. As can be seen, the forward voltage drop of the body diode is rarely influenced by the gate turn-off voltage during the surge current stress. However, the gate turn-off voltage has a significant impact on the I_{dss} of the SiC MOSFET. After a peak surge current of 110 A, the I_{dss} increased by 67 % and 172 % from its initial value at a gate turn-off voltage of -5 V and -10 V, respectively. And the I_{dss} decreased by 73 % from its initial value at a gate turn-off voltage of 0 V.

The gate turn-off voltage has a significant effect on the degradation of threshold voltage and on-state resistance under surge current stress. Fig. 8 shows the evolution of the V_{th} and $R_{ds(on)}$ at different gate turn-off voltage levels after 70A and 110A surge current stress, respectively. After a peak surge current of 70 A, the V_{th} decreases by 4.5 % from its initial value at a gate turn-off voltage of -10 V. However, the variation of V_{th} at a gate turn-off voltage of -5V and 0V condition is small. The reason for the smaller change of V_{th} is the DUTs were only stressed by 100 cycles surge current pulses, while large shift of V_{th} is observed when several thousand cycles surge current stress was applied to the DUTs as detailed in Fig.10. The variation of V_{th} and $R_{ds(on)}$ is more obvious under large surge current stress. After a peak surge current of 110 A, the V_{th} of SiC MOSFET increases by 2.9 % at V_{gs_off} of 0 V, while the V_{th} decreases by 8 % and 17.8 % when the V_{gs_off} decrease to -5 V and -10 V, respectively.



(a) (b)

Fig. 8. (a) Evolution of V_{th} with different gate turn-off voltage after 70A and 110A surge current stress. (b) Evolution of $R_{ds(on)}$ with different gate turn-off voltage after 70A and 110A surge current stress.

The change of on-state resistance shows a similar trend to the threshold voltage because $R_{ds(on)}$ can be affected by the change of V_{th}. The measured on-state resistance of SiC MOSFETs can be influenced by different mechanisms, including chip-related (gate oxide) degradation and package-related (source metallization and bond-wire) degradation [25]. The change of on-state resistance of the SiC MOSFET is mainly induced by the chip-related degradation in this case. This is because the DUTs only subjected to hundreds of surge current pulses stress, which unlikely to trigger the package degradation. The SiC MOSFET chip resistance is mainly comprised of the channel resistance and drift layer resistance. As shown in Fig.7 (a), no obvious degradation of the drift layer resistance is observed under suge current stress because the voltage drop of body diode keeps almost unchanged. In the SiC MOSFETs, the poor quality of the oxide layer and an extraordinary high interface trap density at the SiC/SiO_2 interface result in low channel mobility and therefore high contributions of the channel to the total on-resistance [26]. The channel

resistances strongly depend upon the number of free carriers induced by the gate bias in the inversion layer and the channel mobility along the SiC/SiO_2 surface [27]. The channel resistance R_{ch} can be expressed as:

$$R_{ch} = \frac{L_{ch}}{W \mu_{ni} C_{ox} (V_{gs} - V_{th})} \quad (1)$$

where L_{ch} is the length of the channel, W is the width of the channel, μ_{ni} is the inversion channel mobility for electrons, C_{ox} is the specific capacitance of the oxide and V_{gs} is the gate bias voltage. The L_{ch}, W, and C_{ox} keep constant values. The change of the $R_{ds(on)}$ has a linear correlation to the variation of V_{th}, suggesting that the variation of the channel resistance dominates the degradation of the $R_{ds(on)}$. After a peak surge current of 110 A, the $R_{ds(on)}$ increased by 1.8 % from its initial value at V_{gs_off} of 0 V, while it decreases by 0.5 % and 2.2 % at V_{gs_off} of -5 V and -10 V, respectively.

E. Influence of Surge Current Cycle numbers on Performance Degradation

Surge current stress may occur repetitively in practical applications, and repetitive surge current tests were carried out to identify the device degradation on SiC MOSFETs under long term operation. A peak surge current of 70A (60% of the I_{FSM}) was selected and the DUTs was repeatedly subjected to surge current stress until the device is failed. The static electrical parameters of the SiC MOSFETs are measured after every 1k surge current cycles.

The evolution of the V_{th} and I_{dss} as a function of the number of surge current cycles have been extracted and shown in Fig.9. Severe degradation of the V_{th} and I_{dss} with the accumulation of surge current cycles can be seen at V_{gs_off} of -10 V. The V_{th} decreases by 32% from its initial value in 4k cycles, while the I_{dss} increases to 80μA at 1200V. After 4k surge current cycles, the test SiC MOSFET is failed due to a short-circuit between gate-source terminals. And the blocking voltage of the degraded device has been reduced to 600V due to a large drain leakage current. This can be attributed to higher electrical stress applied on gate oxide with V_{gs_off} of -10 V. On the other hand, the degradation of V_{th} and I_{dss} is much slower at V_{gs_off} of -5 V and 0 V conditions. The V_{th} increases by 7.1 % from its initial value at V_{gs_off} of 0 V after being stressed up to 8k cycles, while it decreases by 6.2 % from its initial value at V_{gs_off} of -5 V. In the meantime, the I_{dss} decreased by 43 % after being stressed up to 8k cycles at V_{gs_off} of 0 V, while the I_{dss} increased by 95 % at V_{gs_off} of -5 V. After 8k surge current cycles, gate-source terminals short-circuit failure was also observed at the devices with V_{gs_off} of -5 V and 0 V condition. The devices still retain a 1200V blocking capability.

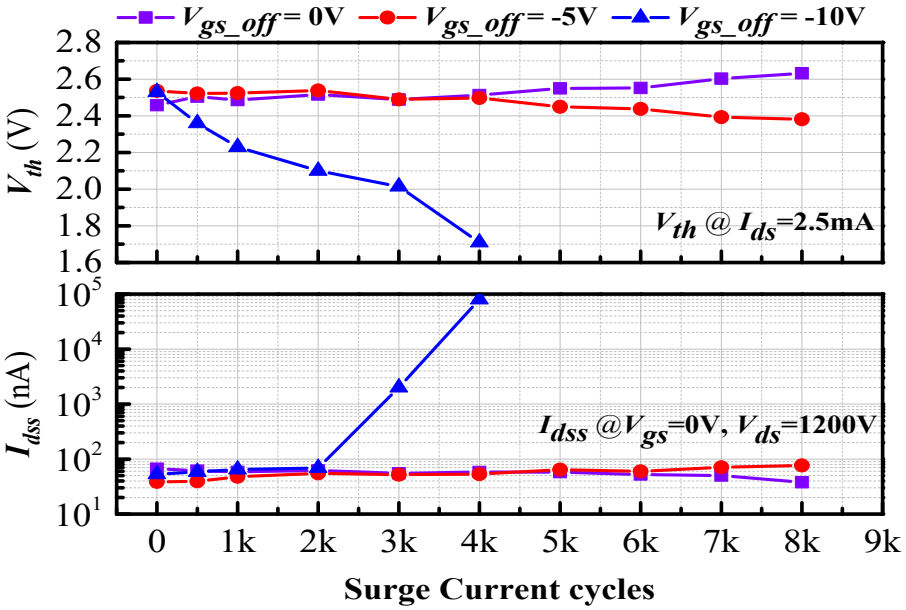


Fig. 9. Evolution of V_{th} and I_{dss} with the accumulation of surge current cycles under 70A surge current stress.

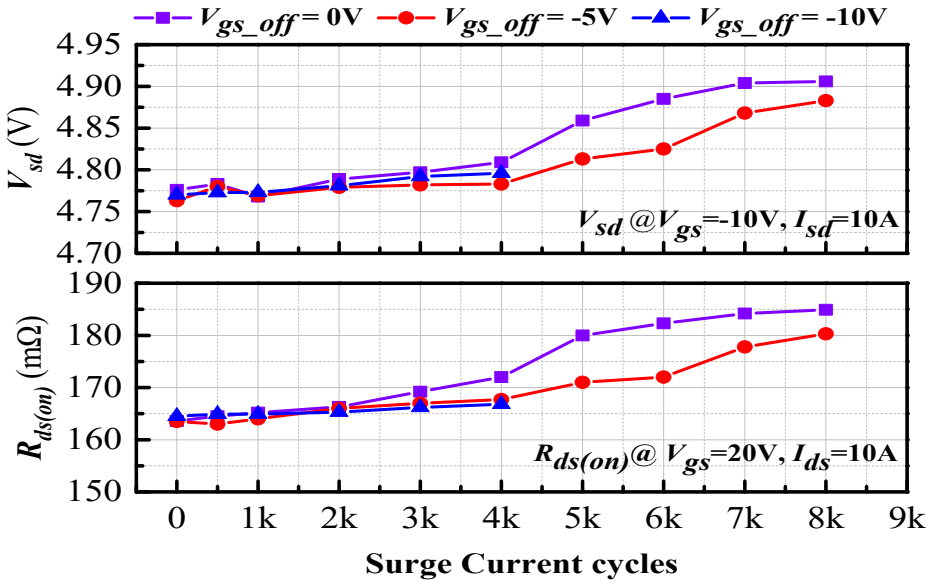


Fig. 10. Evolution of V_{sd} and $R_{ds(on)}$ with the accumulation of surge current cycles under 70A surge current stress.

Both the V_{sd} and $R_{ds(on)}$ show an increasing trend with the increase of surge current cycles as shown in Fig.10. The change of V_{sd} shows a very similar trend to the variation of $R_{ds(on)}$. It is well known that bipolar degradation may happen if the current is conducted in the body-diode forward direction of SiC MOSFET [28]. The stacking faults inside the SiC device act as resistance due to the electrons are trapped in stacking faults that exist in the epitaxial layer. Not only the forward voltage drop of body diode, but also the on-state resistance of SiC MOSFETs degrade.

In order to verify whether the increase of the V_{sd} and $R_{ds(on)}$ was caused by bipolar degradation, double pulse tests were performed after repetitive surge current stress. This is because when bipolar degradation occurs, the stacking faults expand act as recombination centers and therefore, the electron-hole plasma concentration decreases in these regions [29],[30]. The decrease of the total plasma charge in SiC MOSFET can be evaluated by measuring the reverse recovery charge of the SiC MOSFETs in double pulse test. Fig.11 shows the evolution of reverse recovery of the body-diode with the increase of surge current cycles. It shows that the reverse recovery charge and peak reverse-recovery current of the body diode keeps unchanged after repetitive surge current stress. Therefore, the bipolar degradation was unlikely occurs in these DUTs. The increase of V_{sd} and $R_{ds(on)}$ can be attributed to the package degradation resulting from repetitive cyclic thermal stress of the devices [31].

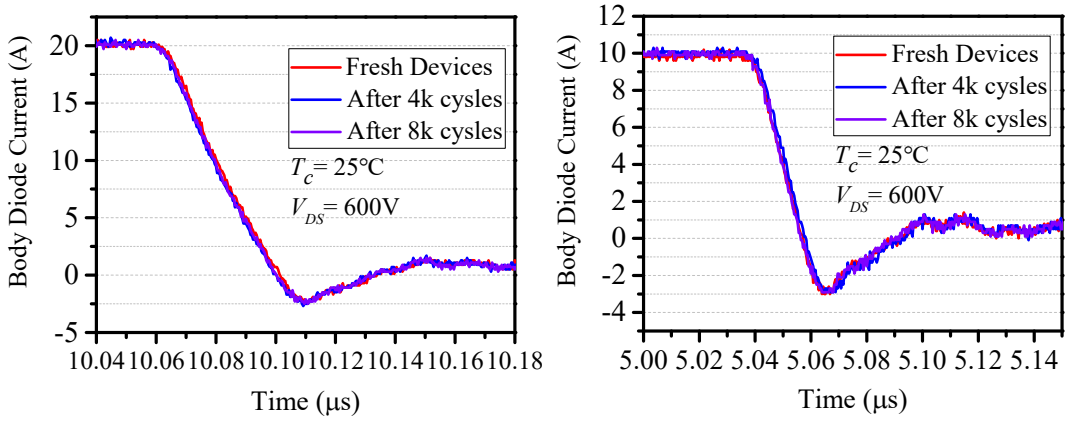


Fig. 11. Evolution of reverse recovery of the body-diode with the accumulation of surge current cycles under 70A surge current stress and V_{gs_off} = -5V.

III. Degradation Mechanism and Experiment Verification

A. *TCAD Simulation and Degradation Mechanism*

In order to verify the physical mechanism behind the gate oxide degradation phenomena under surge current stress of body diode, electro-thermal TCAD simulations were performed to simulate the surge current process of the SiC MOSFET with the same condition. The electro-thermal TCAD simulation model was calibrated to match the behavior of the studied commercial device, and this could be taken as a general case study. Fig.12 shows the current distribution within the SiC MOSFET cell under a peak surge current stress of 110A and 5ms. When a large surge current flows through the body diode of SiC MOSFETs, most of the current vertically flows through the p-body region and n-drift region, while a small portion of current horizontally flows through the p-body to the channel region and JFET region. However, the current flowing through the channel region and JFET region could be affected by the gate turn-off voltage during surge current stress.

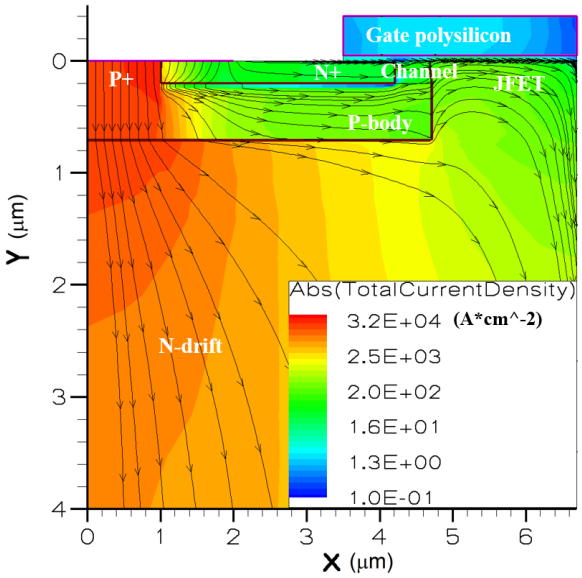


Fig. 12. Surge current conduction paths of simulated SiC MOSFET under 110A surge current stress and 5ms.

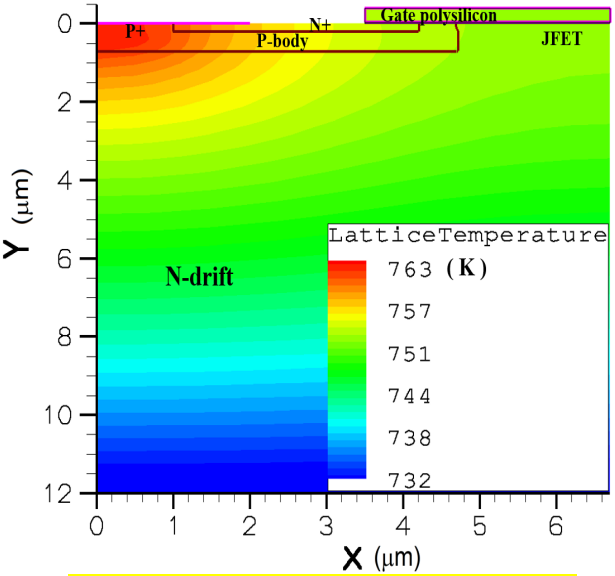


Fig. 13. Temperature distribution of simulated SiC MOSFET cell region under 110A surge current stress and 5ms.

Large surge current induces increasing power dissipation of the SiC MOSFET and rapid increase of junction temperature. Fig.13 shows the temperature distribution within the SiC MOSFET cell under a peak surge current stress of 110A and 5ms. It shows that the highest temperature localized in the P+ region, this is because of large current concentrate at this region under surge current stress. The heat propagates toward the gate oxide and JFET region with the increase of surge current duration time. The temperature at the gate oxide region is approximately ten degrees Celsius lower than the highest temperature point.

The surge current condition of SiC MOSFET's body diode under 110A surge current and different gate turn-off voltage conditions are simulated for comparison. Fig.14 shows the vertical electric field in gate oxide at the interface of SiC and oxide (Y = 0 μm) with different gate turn-off voltage under surge current stress. The positive vertical electrical field direction is defined from the gate oxide layer to the SiC epitaxy layer. SiC planar MOSFETs have two sensitive areas concerning the electric field stress on gate oxide under surge current stress. First, the gate oxide interface above the channel region and second the gate oxide interface above the JFET region. As shown in the figure, the vertical electric field along the SiC/SiO_2 interface shows a continually increase at the channel region (X = 4.2~4.6 μm) and exhibits the uniform peak distributions at the JFET region (X = 4.7~5.5μm). There is an approximately 2.8V internal built-in potential exists in the P-body and N+ junction when the current flows through the body diode. Therefore, the potential of the SiC semiconductor at the channel region and JFET region is lower than that of the source terminal. When the gate turn-off voltage is 0V, a positive vertical electric field exists along the SiC/SiO_2. And this positive electric field decreases close to zero when the gate turn-off voltage decreases to -3V. As the gate turn-off voltage continue decreasing to -5 V and -10 V, the vertical electric field along the SiC/SiO_2 turns from a positive direction to a negative direction.

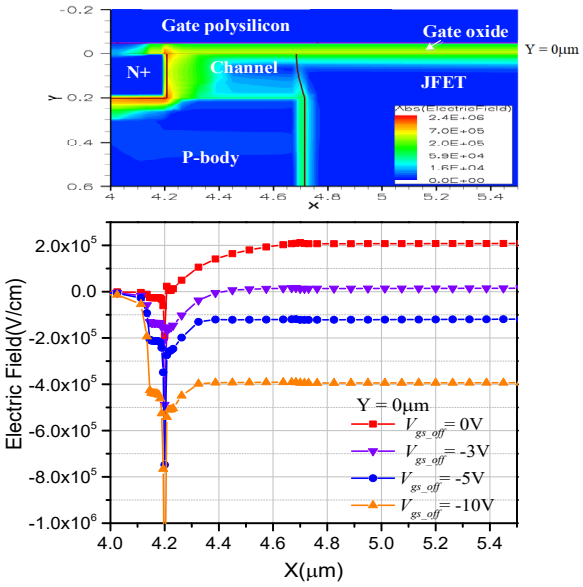
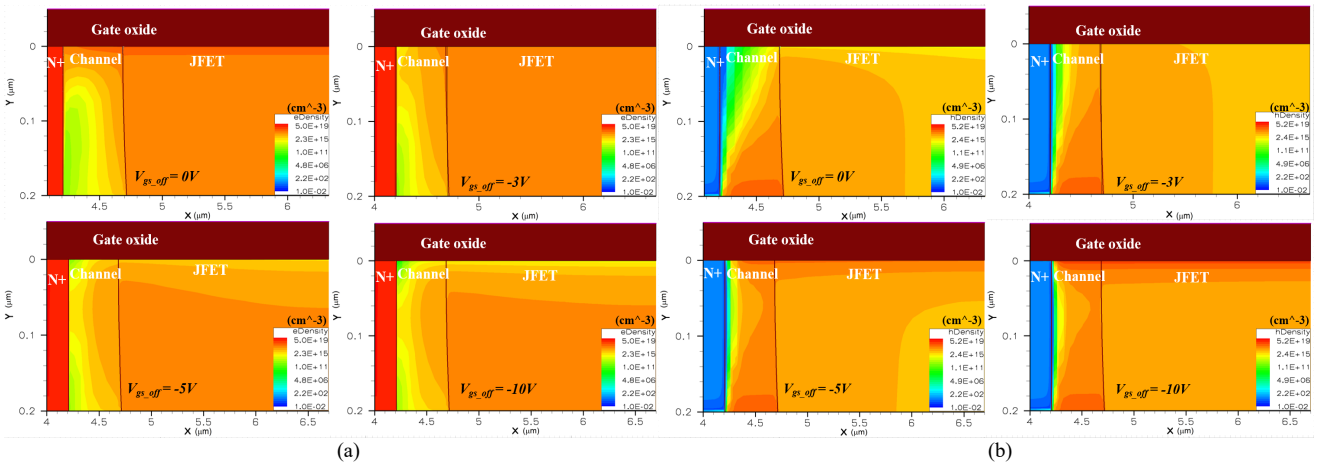


Fig. 14. Vertical electrical field along the SiC/SiO_2 interface of SiC MOSFET cell region with different V_{gs_off} under 110A surge current stress and 5ms.

Fig.15 shows the hole density and electron density along the SiC/SiO_2 interface with different V_{gs_off} under 110A surge current stress and 5ms, respectively. At 0V gate turn-off voltage condition, a large density of electrons accumulated at the SiC/SiO_2 interface due to the channel is partially opened. The positive vertical electric field contributes to the injection of electrons into the gate oxide at the channel region and JFET region. As the gate turn-off voltage decreases, the electron density decreases and holes begin to accumulate along the SiC/SiO_2 interface. Therefore, the negative vertical electric field leads to the holes tunneling into the gate oxide above the channel region and JFET region at gate turn-off voltage of -5V and -10V.



(a) (b)

Fig. 15. Carrier density along the SiC/SiO_2 interface with different V_{gs_off} under 110A surge current stress and 5ms, (a) Electron density (b) Hole density.

The degradations of the V_{th} and I_{dss} of the SiC MOSFETs are due to the presence and accumulation of charge defects in the gate oxide traps during surge current stress. Depending on the surface potential, the oxide traps may be positive or negative charged due to the holes and electrons captured via a direct tunneling mechanism under surge current stress. Fig.16 shows the energy band state of the SiC/SiO_2 structure of SiC MOSFET under surge current stress condition. When the MOS structure enters

into depletion state, the electron and hole densities are both small. At this time, the corresponding gate turn-off voltage is defined as depletion voltage ($V_{depletion}$). When the negative gate turn-off voltage is lower than the $V_{depletion}$, band bending at the surface inducing a large density of holes accumulated at the interface between the gate oxide and the SiC semiconductor. The holes direct tunneling into the gate oxide and begin to build up in the oxide traps. On the one hand, the accumulation of positive holes in the oxide traps increases the effective electric field across the gate oxide in the channel region, so the required threshold voltage to form the MOS inversion channel below the gate oxide decreases. On the other hand, the I_{dss} can be influenced by the trapped holes in the gate oxide above the JFET region due to an increased electrical field at the P-body/N-drift junction in reverse blocking state [32],[33]. Analogously, when the negative gate turn-off voltage is higher than $V_{depletion}$, electrons begin to accumulate at the SiC/SiO_2 interface. Electrons tunneling into gate oxide and accumulated at the oxide traps results in an increase of the V_{th} and decrease of I_{dss}. However, it should be pointed out that the $V_{depletion}$ varies for different manufacture's SiC MOSFET because the design parameter and gate oxide processing technique are different.

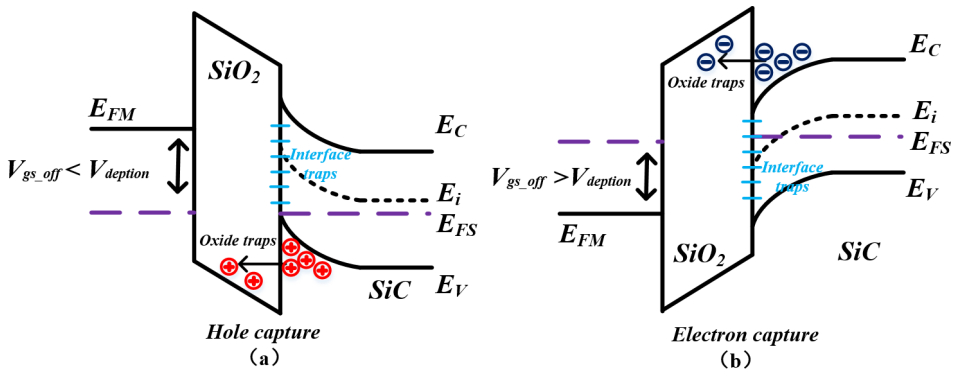


Fig. 16. The influence of gate turn-off voltage on energy band state of SiC/SiO_2 structure of SiC MOSFET under surge current stress. (a) Hole capture, (b) Electron capture

In addition to the gate turn-off voltage, the high junction temperature is another major limiting factor responsible for the gate oxide degradation under surge current stress. Additional gate oxide traps can be generated under high-temperature stress when the SiC MOSFET's body diode is subjected to a large surge current. These active traps can engage in the charge trapping through thermally assisted tunneling and causing severe degradation of the gate oxide [34]-[36]. The junction temperature of SiC MOSFET is related to the amount of power dissipation that the device is subjected to, which is mainly determined by the surge current amplitudes and forward voltage drop of the body diode under surge current stress.

B. *Experiment Verification*

In order to verify the influence of gate turn-off voltages and junction temperature on the gate oxide degradation of SiC MOSFET under surge current stress, the generation and accumulation of charges in the gate oxide traps are verified through

measuring the variation of subthreshold characteristics, C-V characteristics before and after the surge current stress. High temperature recovery treatment of the stressed device was also carried out.

The variation of near-interface oxide traps density under surge current stress can be substantiated by the forward and backward I_d-V_{gs} sweep measurement of SiC MOSFET. Fig. 17 shows the measured I_d-V_{gs} characteristics of SiC MOSFETs at room temperature after surge current stress. The gate voltage V_{gs} starting sweep at a negative gate bias of -10V to V_{gs} =10V (up-sweep, solid lines) and from V_{gs} =10V back to a negative bias of -10V (down-sweep, dotted lines) at a drain voltage of V_{ds} = 0.1V. Since the currents involved are small, the DC static mode was employed in the measurement. The SiC MOSFET's subthreshold curve exhibited a large clockwise hysteresis because the oxide traps capture electrons during the up-sweep measurement and cannot emit electrons during the down sweep measurement due to a relatively long emission time constant [37], [38]. It can be observed that the hysteresis envelops I_d-V_{gs} curves overall shift toward a negative direction with the increase of surge current stress due to the holes being trapped in the gate oxide traps.

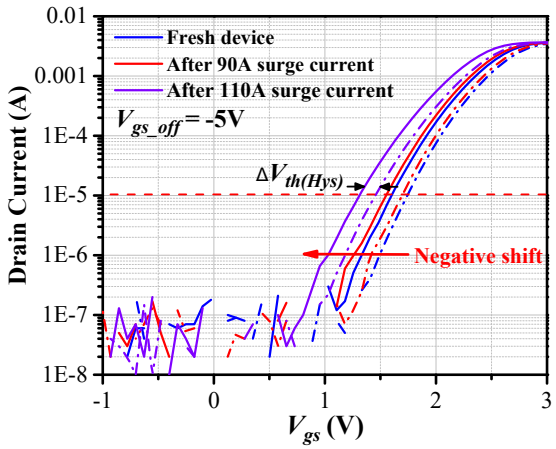


Fig. 17. Transfer characteristics of SiC MOSFET in the subthreshold regime with the increase of surge current under V_{gs_off} = -5V.

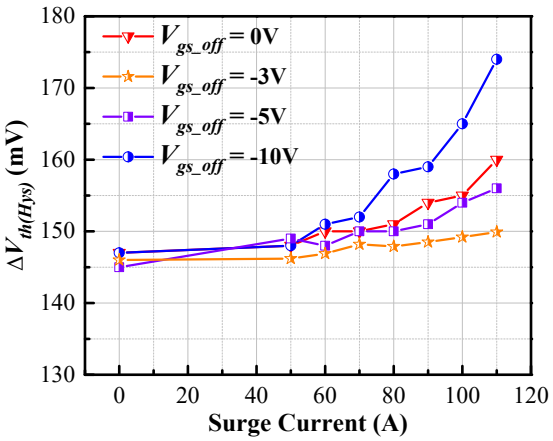


Fig. 18. Variation of the oxide traps density (ΔV_{th} *(Hys)*) in SiC MOSFETs with the increase of surge current.

The subthreshold hysteresis ΔV_{th} (*Hys*) was defined as the difference of the gate voltage of the up-sweep trace and the gate voltage of the down-sweep trace, both at I_d =1e^{-5}A. The ΔV_{th} (*Hys*) is associated with the near-interface oxide traps density. The dependence of the ΔV_{th} (*Hys*) on the gate turn-off voltage under different surge current stress is shown in Fig. 18. ΔV_{th} (*Hys*) showed an increasing trend in line with the surge current. It is because the junction temperature increases with the surge current amplitude. After a peak surge current of 110A, the ΔV_{th} (*Hys*) increased by 13mV, 5mV, 11mV and 27mV at the gate turn-off voltage of 0V,-3V, -5V and -10V, respectively. This indicates that the generation of active oxide traps has a linear correlation to the variation of V_{th} and I_{dss} under surge current stress.

The types and distribution of the charges injected into the gate oxide under surge current stress can be distinguished by the shifts of the C_g-V_{gs} curve after the surge current stress, which indicates the sites and regions of SiC/SiO_2 interfacial damage. The degradation of C_g-V_{gs} characteristics under different surge current stress at V_{gs_off} of -5V is shown in the Fig.19. A 1 MHz, AC signal of 25 mV amplitude was superposed to the DC sweep voltage of the SiC MOSFET in order to measure its capacitance, and the device's drain terminal is shorted to the source terminal. An apparent negative shift of C_g-V_{gs} curves can be seen when the gate voltage V_{gs} is in the range from -7V to -5V, and the shifting trend is more obvious with the increase of surge current amplitude. This can be explained by the holes injection into the gate oxide along with the interface above the JFET region [38]. Moreover, a significant negative shift of C_g-V_{gs} curves were also observed in the range from -2V to 1V, and this is attributed to the injection of holes into the gate oxide along with the interface above the channel region. The accumulation of positive holes in oxide attracts electrons in the SiC layer along with the bottom oxide interface, reduces the thickness of the depletion layer beneath the bottom of the gate and therefore increases the depletion capacitance.

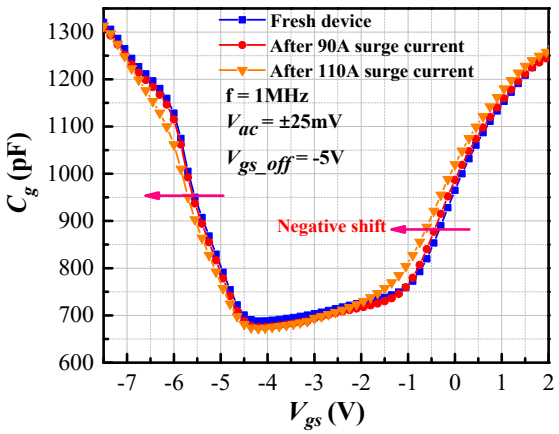


Fig. 19. Measured C_g-V_{gs} curves of the SiC MOSFET after different surge current stress of body diode under V_{gs_off} of -5 V.

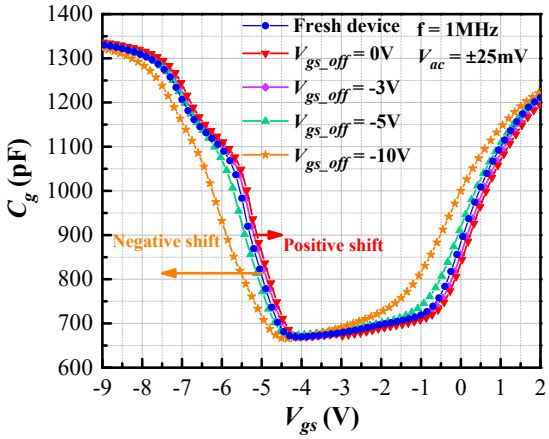


Fig. 20. Measured C_g-V_{gs} curves of SiC MOSFET before and after a peak surge current of 110A with different V_{gs_off}.

The degradation of C_g-V_{gs} characteristic after the surge current stress at different gate turn-off voltages are depicted in the Fig.20. It can be seen that the hole tunneling effect is more obvious with the decrease of negative gate turn-off voltage, especially at -10V gate turn-off voltage condition. However, the C_g-V_{gs} curves show a positive shift at 0V gate turn-off voltage condition. This is due to surge current stress leads to the injection of electrons into the gate oxide traps above the channel region and JFET region. Furthermore, the C_g-V_{gs} curve shows a slightly positive shift with the surge current stress with -3V gate turn-off voltage.

The high-temperature recovery test has been carried out to validate the gate oxide degradation of the degraded SiC MOSFET. The high-temperature can provide activation energy to release the trapped holes from the gate oxide traps [39]. Following a succession of surge current stress with a peak surge current of 110A at -5V gate turn-off voltage, the degraded SiC MOSFET was

kept at the ambient temperature of 150 °C in a thermostat to check its possible high-temperature recovery. And the device is characterized at 150 °C after the different high temperature recovery time. Fig. 21 shows the evolution of the normalized V_{th} and $R_{ds(on)}$ of the degraded device at 150 °C versus recovery time, respectively. When the high temperature recovery time increases, both the V_{th} and I_{dss} slightly move toward the initial value of the fresh die. Furthermore, the C_g-V_{gs} curve of the SiC MOSFET after high temperature treatment also exhibit a slight shift to its initial value.

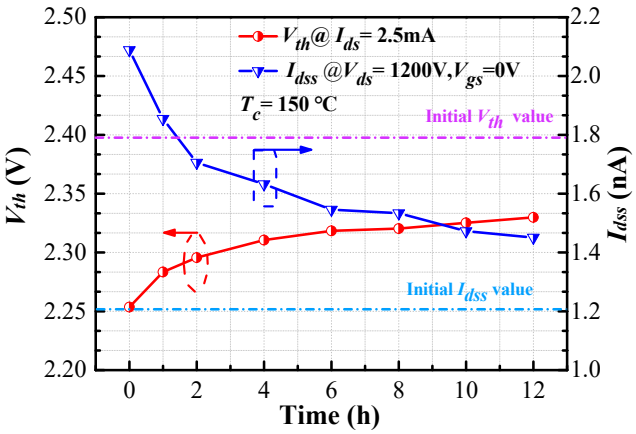


Fig. 21. Variations of normalized V_{th} and I_{dss} as a function of recovery time under 150°C temperature.

IV. Mitigation Technique with Optimal Gate Turn-off Voltage

It was observed from the experiment results that the I_{FSM} of the body diode of planar gate SiC MOSFETs is independent of the gate turn-off voltage, while the gate turn-off voltage exhibits a strong influence on the degradation of SiC MOSFET and the corresponding electrical parameter deviation when the body diode is subject to the repetitive surge current stress. Based on the analysis of the degradation mechanism, the gate oxide degradation can be suppressed by reducing the gate oxide trap density and selecting optimal gate turn-off voltage. From the device design and fabrication point of view, the forward voltage of body diode under the surge current condition should be as small as possible in order to avoid an immense amount of heat accumulation on the device during surge current stress. This is particularly important since the oxide layer of SiC MOSFET is susceptible to over-temperature stress, which may lead to an increase of local defects within the gate oxide and SiC/SiO_2 interface. Furthermore, SiC/SiO_2 interface state density can be adequately reduced by suitable passivation process conditions [40]. Since fewer oxide traps are activated during the high-temperature stress to participate in the trapping process, the variation of electrical parameters induced by charges trapping can be greatly reduced. From the gate control point of view, it may be advantageous to have a proper gate turn-off voltage to achieve a high gate oxide reliability and a low forward voltage drop of the body diode when using the body diode. The charge tunneling phenomenon is sensitive to the electrical potential applied on the gate oxide. According to the

results shown in section II, a high electric field in the gate oxide during surge current stress can potentially accelerate the wear out of the gate oxide. An inappropriate turn-off voltage could be considered as a long-term reliability risk, in particular concerning the high defect density in the SiC/SiO_2 interface of SiC MOSFETs.

In order to improve the surge current reliability of the body diode of the SiC MOSFET, the amplitude of the surge current should be limited to alleviate the thermal stress on gate oxide and prevent package degradation under repetitive surge current stress. Meanwhile, the gate turn-off voltage of SiC MOSFET should be selected appropriately to reduce the gate oxide degradation induced by the possible surge current stress. According to the energy band state of SiC/SiO_2 structure of SiC MOSFET, as shown in Fig.16, when the gate turn-off voltage is close to -3 V, there is a weak electrical field along the SiC/SiO_2 interface, which alleviates the charge tunneling effect of the gate oxide. Fig. 22 shows the evolution of the V_{th} and I_{dss} as a function of gate turn-off voltage after a surge current of 110A. The variation of the V_{th} and I_{dss} of the SiC MOSFET exhibit a strong relationship with the gate turn-off voltage under surge current stress. More specific, both V_{th} and I_{dss} show little variation at -3V gate bias. Therefore, an optimal gate turn-off gate voltage of -3V is suggested to suppressing the device degradation when using the body diode. However, it should be noted that the differences in SiC MOSFET's cell structure, design parameter, and processing technique may result in different optimal V_{gs_off}.

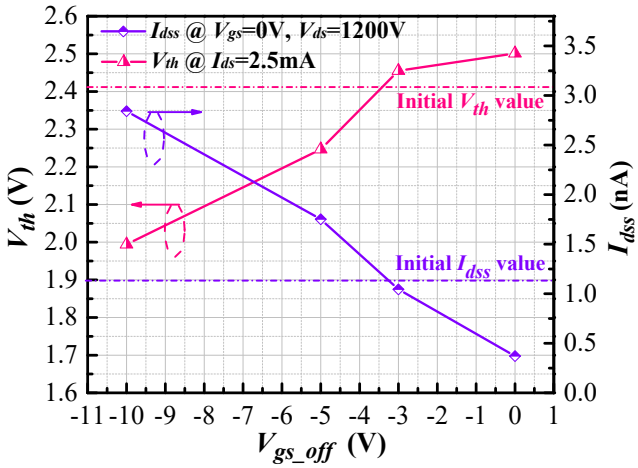


Fig. 22. Variations of normalized V_{th} and I_{dss} as a function of gate turn-off voltage after surge current stress.

V. Conclusion

In this paper, the degradation phenomenon of the 1200V planar gate SiC MOSFET under repetitive surge current stress of the body diode is investigated. Degradation mechanism of the device under surge current stress is experimentally verified and the mitigation techniques to suppress device degradation are discussed. The key points of this paper can be summarized as follows.

1) After a large surge current stress for the selected 1200V commercial planar gate SiC MOSFET, the forward voltage drop of body diode shows a minor change, while an obvious change in V_{th} and I_{dss} was observed. This indicates significant degradation of the gate oxide of SiC MOSFETs. The growth of stacking faults in SiC MOSFET has not been observed after surge current stress by analyzing the reverse recovery characteristic of the degraded devices.

2) The surge current amplitude and the gate turn-off voltage exhibit a strong influence on the degradation of SiC MOSFETs under surge current stress. The electrical parameters degradation of SiC MOSFETs at 110A surge current condition is more severe than 70A surge current condition. After a peak surge current of 110 A, the V_{th} of SiC MOSFET decreases by 8 % and 17.8 % when the V_{gs_off} decreases to -5 V and -10 V, respectively. The increase of $R_{ds(on)}$ and V_{sd} after thousands of repetitive surge current cycles are attributed to package-related degradation under repetitive cyclic thermal stress.

3) The high electrical field applied on the gate oxide in addition to the high junction temperature under surge current stress are the main reasons responsible for the gate oxide degradation. The charges inject and being trapped in the gate oxide traps cause the gate oxide degradation of SiC MOSFET. Holes trapped in the gate oxide traps at a gate turn-off voltage of -5V and -10V condition, which induces a decrease of the V_{th} and increase of I_{dss}. When the gate turn-off voltage is 0V, the electrons trapped in the gate oxide traps induces an increase of the V_{th} and decrease of I_{dss} under surge current stress.

5) The subthreshold voltage characteristics show the additional oxide traps are generated with the increase of surge current, and the increase of gate oxide trap density is consistent with the variations of the V_{th} and I_{dss} under the surge current stress. Capacitance-voltage measurement results show that the injection of holes occurs within the gate oxide traps above the channel region and JFET region. The degradation of the SiC MOSFET's electrical performance can be partially recovered under high-temperature treatment. It means that some trapped holes within the gate oxide traps are released at high temperature.

6) Based on the degradation mechanisms, an optimal negative gate turn-off voltage of -3V was suggested to suppress the gate oxide degradation of the SiC MOSFET under repetitive surge current stress in this case study.

REFERENCES

[1] X. She, A. Q. Huang, Ó. Lucía and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8193-8205, Oct. 2017.

[2] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang and Y. Zhang, "Performance Evaluation of High-Power SiC MOSFET Modules in Comparison to Si IGBT Modules," in *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1181-1196, Feb. 2019.

[3] PowerAmerica, "Poweramerica strategic roadmap for next generation wide bandgap power electronics," 2017. [Online]. Available: https://www.poweramericainstitute.org

[4] S. Yin, Y. Liu, Y. Liu, K. J. Tseng, J. Pou and R. Simanjorang, "Comparison of SiC Voltage Source Inverters Using Synchronous Rectification and Freewheeling Diode," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1051-1061, Feb. 2018.

[5] K. Yamaguchi, K. Katsura, T. Yamada and Y. Sato, "Criteria for Using Antiparallel SiC SBDs with SiC MOSFETs for SiC-based Inverters," in *IEEE Transactions on Power Electronics*. doi: 10.1109/TPEL.2019.2911988.

[6] A. E. Awwad and S. Dieckerhoff, "Operation of planar and trench SiC MOSFETs in a 10kW DC/DC converter analyzing the impact of the body diode," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 917-924.

[7] R. Horff, A. März, M. Lechler and M. Bakran, "Optimised switching of a SiC MOSFET in a VSI using the body diode and additional Schottky barrier diode," in *Proc.17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Geneva, 2015, pp. 1-11.

[8] Z. Wang, J. Zhang, X. Wu and K. Sheng, "Evaluation of reverse recovery characteristic of silicon carbide metal–oxide–semiconductor field-effect transistor intrinsic diode," in *IET Power Electronics*, vol. 9, no. 5, pp. 969-976, 204, 2016.

[9] A. Agarwal, H. Fatima, S. Haney and S. H. Ryu, "A New Degradation Mechanism in High-Voltage SiC Power MOSFETs," in *IEEE Electron Device Letters*, vol. 28, no. 7, pp. 587-589, July 2007.

[10] T. Kimoto, A. Iijima, H. Tsuchida, et al., "Understanding and reduction of degradation phenomena in SiC power devices," in *Proc. IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, 2017, pp. 2A-1.1-2A-1.7.

[11] B. Hull, S. Allen, Q. Zhang, D. Gajewski, et al., "Reliability and stability of SiC power MOSFETs and next-generation SiC MOSFETs," in *Proc. IEEE Workshop on Wide Bandgap Power Devices and Applications*, Knoxville, TN, 2014, pp. 139-142.

[12] A. Bolotnikov, J. Glaser, J. Nasadoski, P. Losee, S. Klopman, A. Permuy, L. Stevanovic, "Utilization of SiC MOSFET body diode in hard switching applications," *Materials Science Forum*, Vols. 778-780, pp. 947-950, 2014.

[13] B.Heinze, J. Lutz, M. Neumeister, R. Rupp and M. Holz, "Surge Current Ruggedness of Silicon Carbide Schottky- and Merged-PiN-Schottky Diodes," in *Proc. International Symposium on Power Semiconductor Devices and IC's*, Orlando, FL, 2008, pp. 245-248.

[14] D. Sadik, S. Heinig, K. Jacobs, et al., "Investigation of the surge current capability of the body diode of SiC MOSFETs for HVDC applications," in *Proc. European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Karlsruhe, 2016, pp. 1-10.

[15] F. Carastro, J. Mari, T. Zoels, B. Rowden, P. Losee and L. Stevanovic, "Investigation on diode surge forward current ruggedness of Si and SiC power modules," in *Proc. European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Karlsruhe, 2016, pp. 1-10.

[16] X. Jiang, D. Zhai, J. Chen et al., "Comparison Study of Surge Current Capability of Body Diode of SiC MOSFET and SiC Schottky Diode," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 845-849.

[17] P. Hofstetter and M. Bakran, "Comparison of the Surge Current Ruggedness between the Body Diode of SiC MOSFETs and Si Diodes for IGBT," CIPS 2018; 10th International Conference on Integrated Power Electronics Systems, Stuttgart, Germany, 2018, pp. 1-7.

[18] P. Hofstetter and M. Bakran, "Predicting Failure of SiC MOSFETs under Short Circuit and Surge Current Conditions with a Single Thermal Model," 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), Riga, 2018, pp. P.1-P.9.

[19] L. Huan, J. Wang, N. Ren, H. Xu, K. Sheng. "Investigation of 1200 V SiC MOSFETs' Surge Reliability." in *Micromachines*, vol.10, no.7, pp.485, 2019.

[20] IXYS, IXGK120N120A3-silicon power IGBT datasheet, 2009, available online at http://www.ixyspower.com/

[21] JEDEC JSD282-B Rev.01, "Silicon Rectifier Diodes," Section 4.2, 2002.

[22] Cree, C2M0160120D-silicon carbide power MOSFET datasheet, 2018, available online at http://www.wolfspeed.com/

[23] J. Lutz, H. Schlangenotto, U. Scheuermann, R. De Doncker, Semiconductor Power Devices. Physics, Characteristics, Reliability, 2nd ed., Springer, 2018.

[24] V. Uhnevionak, A. Burenkov, C. Strenger, et al, "Comprehensive Study of the Electron Scattering Mechanisms in 4H-SiC MOSFETs," in *IEEE Transactions on Electron Devices*, vol. 62, no. 8, pp. 2562-2570, Aug. 2015.

[25] H. Luo, F. Iannuzzo, F. Blaabjerg, W. Li and X. He, "Separation test method for investigation of current density effects on bond wires of SiC power MOSFET modules," *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, Beijing, 2017, pp. 1525-1530.

[26] J. O. Gonzalez and O. Alatise, "Impact of the Gate Oxide Reliability of SiC MOSFETs on the Junction Temperature Estimation Using Temperature Sensitive Electrical Parameters," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 837-844.

[27] B. J. Baliga, Fundamentals of Power Semiconductor Devices. Springer Science & Business Media, 2010.

[28] R. Fujita, K. Tani, K. Konishi and A. Shima, "Failure of Switching Operation of SiC-MOSFETs and Effects of Stacking Faults on Safe Operation Area," in IEEE Transactions on Electron Devices, vol. 65, no. 10, pp. 4448-4454, Oct. 2018.

[29] F. Hoffmann, V. Soler, A. Mihaila and N. Kaminski, "Power Cycling Test on 3.3kV SiC MOSFETs and the Effects of Bipolar Degradation on the Temperature Estimation by VSD-Method," 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 2019, pp. 147-150.

[30] P. Brosselard, A. Perez. Tomas, N. Camara, et al., "The effect of the temperature on the Bipolar Degradation of 3.3 kV 4H-SiC PiN diodes," 2008 20th International Symposium on Power Semiconductor Devices and IC's, Orlando, FL, 2008, pp. 237-240.

[31] E. Ugur, F. Yang, S. Pu, S. Zhao and B. Akin, "Degradation Assessment and Precursor Identification for SiC MOSFETs Under High Temp Cycling," in *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 2858-2867, May-June 2019.

[32] L. Yang, A. Castellazzi, "High temperature gate-bias and reverse-bias tests on SiC MOSFETs", *Microelectronics Reliability*, vol. 53, pp. 1771, 2013.

[33] S. Liu, C. Gu, J. Wei, Q. Qian, W. Sun and A. Q. Huang, "Repetitive Unclamped-Inductive-Switching-Induced Electrical Parameters Degradations and Simulation Optimizations for 4H-SiC MOSFETs," in *IEEE Transactions on Electron Devices*, vol. 63, no. 11, pp. 4331-4338, Nov. 2016.

[34] T. Aichinger, G. Rescher, G. Pobegen, "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs", *Microelectronics Reliability*, vol.80, pp.68-78, 2018.

[35] A. J. Lelis, D. Habersat, R. Green, A, Ogunniyi, M. Gurfinkel, J. Suehle, N. Goldsman, "Time Dependence of Bias-Stress-Induced SiC MOSFET Threshold-Voltage Instability Measurements," in *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 1835-1840, Aug. 2008.

[36] R. Green, A. Lelis, and D. Habersat, "Threshold-voltage bias-temperature instability in commercially-available SiC MOSFETs." *Japanese Journal of Applied Physics*, vol.55, no.4S, 2016.

[37] B. Asllani, H. Morel, D. Planson, A. Fayyaz and A. Castellazzi, "SiC power MOSFETs Threshold-voltage hysteresis and its impact on Short Circuit operation," in *Proc. IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*, Nottingham, United Kingdom, 2018, pp. 1-7.

[38] J. Wei, S. Liu, R. Ye, X. Chen, H. Song, W. Sun, W. Su, S. Ma, Y. Liu, and F. Lin, "Interfacial Damage Extraction Method for SiC Power MOSFETs Based on C-V Characteristics," in *Proc. International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, Sapporo, May. 2017, pp. 359-362.

[39] X. Zhou, H. Su, R. Yue, G. Dai, J. Li, Y. Wang, and Z. Yu, "A Deep Insight Into the Degradation of 1.2-kV 4H-SiC mosfets Under Repetitive Unclamped Inductive Switching Stresses," in *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5251-5261, June 2018.

[40] H. Yano, N. Kanafuji, A. Osawa, T. Hatayama and T. Fuyuki, "Threshold Voltage Instability in 4H-SiC MOSFETs With Phosphorus-Doped and Nitrided Gate Oxides," in *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 324-332, Feb. 2015.